VDINT

Basic BT.656 Video Deinterlacer IP Megafunction

This deinterlacer IP megafunction converts a standard interlaced video stream to progressive video format for further processing or display. Extremely efficient, the deinterlacer megafunction requires little area and transforms the video with practically no delay.

The megafunction implements the most popular basic deinterlacing algorithm, Bob with scan line interpolation. It accepts an industry-standard ITU-R BT.656 interlaced video stream (8-bit 4:2:2 video data mixed with audio, control, and other signals) which may optionally include user-defined SAV codes.

The BT.656 input video is typically 480i/576i, but higher resolutions are possible (requiring higher clock frequencies). The output video contains twice the pixels and has a frame rating matching the input's field rate. Additionally, the user can constrain the possible maximum horizontal resolution with a pre-synthesis parameter.

The deinterlacer megafunction's synchronous control interface allows for easy integration with the system CPU via the address and data buses. The megafunction's efficiency and small size contribute to significant power savings compared to more complex deinterlacers.

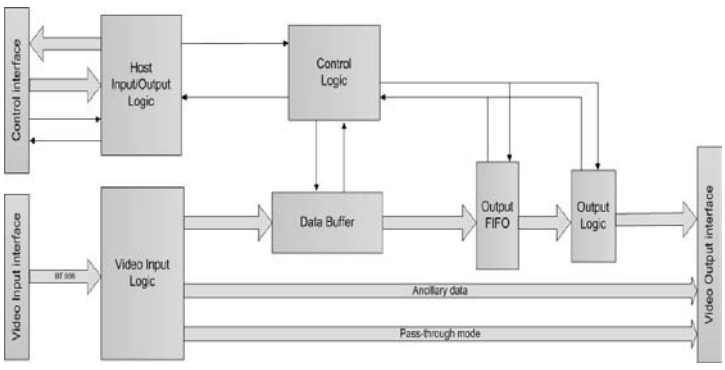
Developed for easy reuse in FPGA or ASIC applications, the megafunction is available optimized for several technologies, with competitive utilization and performance characteristics.

Applications

The VDINT Video Deinterlacer Megafunction is appropriate for a variety of serial communication applications including:

- DVD Players
- AV Receivers
- DTVs
- Surveillance systems

Block Diagram



Features

- Accepts an 8-bit, 4:2:2, YCrCr, video data stream in ITU Recommendation BT.656 video format
- Supports NTSC, PAL, 1080i and all lower resolutions transmitted in conformance with the BT.656 format
- Sophisticated BT.656 analyzer splits contents of the incoming video stream
- Works with optional user-defined SAV (Start of Active Video) codes in the incoming video stream
- Output frame rate equals the input field rate
- Maximum horizontal resolution can be set as a pre-synthesis parameter to reduce logic resources
- Includes write-through mode
- Produces raster scan format of output video data
- Minimum system clock speed equals two times the raw pixel clock speed
- Fully synchronous design: all inputs and outputs are based on the rising edge of clock
- Includes complete documentation and testbench

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Functional Description

The megafunction includes six major blocks, as shown in the block diagram and described below. All the megafunction's inputs and outputs are fully synchronous to the rising edge of the CLK input.

Host Input/Output Logic

Handles communication with the processor side of the system. Manages all writing and reading of internal registers.

Video Input Logic

Splits the incoming BT.656 media stream into video and auxiliary data. The incoming media stream can be 576i/480i or any other resolution complying with the BT.656 format.

Data Buffer

Includes two FIFO modules that store the pixel values needed for the proper implementation of the deinterlacing algorithm. Also includes the computation logic.

Control Logic

Controls all logic modules according to the implemented deinterlacing algorithm. Includes a state machine responsible for the correct data processing and computation. Also incorporates the register logic which stores the user configuration

Output FIFO

Receives and buffers the computed deinterlaced video steam.

Output Logic

Handles the Output FIFO reading and formatting of the outgoing video stream. Also allows the user to stop the megafunction's data processing in case of data overflow at the user's side.

Support

The megafunction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The megafunction has been verified through extensive simulation and rigorous code coverage measurements.

Implementation Results

Reference designs have been evaluated in a variety of technologies.

The following are sample Altera results optimized for speed with buffers set to maximum Horizontal Resolution of 720 pixels.

Altera Devices	ALUTs	Special Features	Frequency (MHz)
Cyclone-3	1,054 LUTs	8 M9Ks	191
Stratix -2 S60-3	773	16 M4Ks	238
Stratix-3 SE110-2	663	8 M9K	212
Stratix-4 GX290-2	627	8 M9K	304

Deliverables

The megafunction is available in ASIC (synthesizable) or FPGA (netlist) forms, and includes everything required for successful implementation. The Altera version includes

- Post-synthesis EDIF netlist
- Sophisticated HDL Testbench (self-checking)
- Simulation scripts, stimulus vectors, test clips, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide

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