H264-MP-E
H.264/AVC HD & ED Video Encoder Core

Implements a hardware H.264 video encoder that supports the ISO/IEC 14496-10/ITU-T H.264 Main Profile specification.

The Main Profile H.264 Encoder Core supports real-time encoding of 4:2:0 video with 8-bits per color sample, and provides performance up to Level 5.2. An Intra-only encoder variation features extremely low, sub-frame latency, can operate without an external memory and requires half the silicon resources.

The core provides great quality for all types of video and transmission bit rates. Under Constant Bit Rate mode (CBR), it preserves uniform quality while respecting the bit rate—even for the most challenging video content—by making multiple quantization adjustments within a single frame and by selecting the encoding mode based on runtime adaptive models. This allows the core to rapidly adapt to inter- and intra-frame video content variations and the output stream to comply with the hypothetical reference decoder’s coded-picture buffer (HRD-CPB) requirements of the H.264 spec, ensuring uninterrupted video decoding.

The encoder is designed for easy integration. It operates independently of the system processor and features simple interfaces that make system integration straightforward. Furthermore, the core works with any type of external memory and memory controller devices via a flexible external memory interface. Best-practice RTL coding and high-quality deliverables, tested and proven in dozens of designs, ensure that no bad surprises will arise from verification through FPGA or ASIC technology mapping.

Applications
The H264-MP-E core efficiently handles extended definition (ED) through high definition (HD) video, and is suitable for a range of applications including surveillance and monitoring, video conferencing, and streaming video on demand.

Block Diagram
Features Continued

Encoding Tools
- CABAC or CAVLC Encoding
- Motion Estimation
  - Optimal, Full-Search
  - 32x20 or higher search area; down to ¼ pel accuracy
  - Variable block size; up to four motion vectors per MB
- Sophisticated block skipping for fewer motion artifacts in low bit rates
- All 16x16 and 4x4 luma, and all chroma intra prediction modes
- In-Loop deblocking filter
- Multiple slices for error resilience
- Optional thresholding of quantized transform coefficients

Implementation Results

H264-MP-E reference designs have been evaluated in a variety of technologies. The following are ASIC, pre-layout, results for H264-MP-E core, reported from synthesis tool and silicon vendor design kit under worst case conditions. Internal memory figures are given for video sequences with resolution up to 1920x1080.

<table>
<thead>
<tr>
<th>ASIC Technology</th>
<th>Eq. NAND2 gates</th>
<th>Fmax (MHz)</th>
<th>Throughput (MPixels/s)</th>
<th>Memory (kbits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC 90nm</td>
<td>600 K</td>
<td>333</td>
<td>136</td>
<td>725</td>
</tr>
</tbody>
</table>

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:
- HDL (VHDL or Verilog-2001) RTL source code.
- Sophisticated self-checking Testbench Synthesis scripts.
- Simulation script, vectors and expected results.
- Software (C++) Bit-Accurate Model and test-vector generator
- Comprehensive user documentation, including detailed specifications and a system integration guide.

Evaluation

The video encoder’s extremely high visual quality is best evaluated by compressing examples of an application’s actual input video. There are three ways to do this.
- Work directly with CAST’s video compression engineers,
- Use the available BAM for software simulation, or
- Use the available H264-AP H.264 Application Platform, a board and software package combining the H.264 Encoder, memory and controller, and other IP cores with software drivers and a graphical user interface for H.264 control.

Please contact CAST Sales to discuss your specific project requirements (sales@cast-inc.com) (+1 201.391.8300).

H.264 Encoders Family

A family of H.264 encoder cores is available from CAST. The following table outlines the family members and their basic features.

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Slice type(s)</td>
<td>IDR, P</td>
<td>IDR</td>
<td>IDR, P</td>
<td>IDR</td>
<td>IDR, P</td>
<td>IDR</td>
</tr>
<tr>
<td>Chroma format(s)</td>
<td>4:2:0</td>
<td>4:2:0</td>
<td>4:2:0</td>
<td>4:2:0</td>
<td>4:2:0, 4:2:2</td>
<td>4:2:0, 4:2:2</td>
</tr>
<tr>
<td>Sample depth (bits)</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8, 10, 12</td>
<td>8, 10, 12</td>
</tr>
<tr>
<td>CAVLC / CABAC</td>
<td>✓ / x</td>
<td>✓ / x</td>
<td>✓ / ✓</td>
<td>✓ / ✓</td>
<td>✓ / ✓</td>
<td>✓ / ✓</td>
</tr>
<tr>
<td>Rate control (CBR &amp; CQP-VBR) with separate Luma / Chroma QP control</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>AVC-Intra 50 / 100 / Ultra suitability</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Throughput (clocks/pixel)</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5 - 2.75</td>
<td>2.5 - 2.75</td>
</tr>
<tr>
<td>Sub-frame latency capable</td>
<td>x</td>
<td>✓</td>
<td>x</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

Note 1: 4:4:4 profiles support 12bits for 4:2:0 or 4:2:2

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The H264-MP-E core is sourced from Technology Partner Alma Technologies.