

CAST

H264-MP-E

H.264/AVC HD & ED Video Encoder Core

Features

H.264 Video Encoding

- Fully compliant to the ISO/IEC 14496-10/ITU-T H.264 main specification (MPEG-4 Part 10, Advanced Video Coding)
- Profile level up to 5.1
- Flexible 4:2:0 video input
 - Planar scan
 - Interleaved scan
 - Macroblock scan
- Produces a ITU-T H.264 Annex B compliant NAL video byte stream
- Compression efficiency from QCIF up to HD resolutions
- Programmable bit rate control
 - Constant bit rate compression
 - Constant-Qp compression
- Single reference frame
- Advanced Inter-Prediction
 - Quarter pel accuracy
 - Variable block size
 - Block skipping
 - Up to 32x20 search area
- Advanced intra prediction modes
 - All four Intra 16x16 luma prediction modes
 - All four Intra prediction 8x8 chroma modes
 - All nine Intra 4x4 luma prediction modes
- Advanced Intra prediction in Inter slices
- Multiple slices for enhanced error resilience
- Advanced mode selection for superior compression and quality
- CABAC or CAVLC Encoding
- In-Loop deblocking filter
- Optional Intra-only coding

This H.264 IP core implements a video encoder compatible to the Main profile of the H.264 standard, also known as MPEG-4 Part 10.

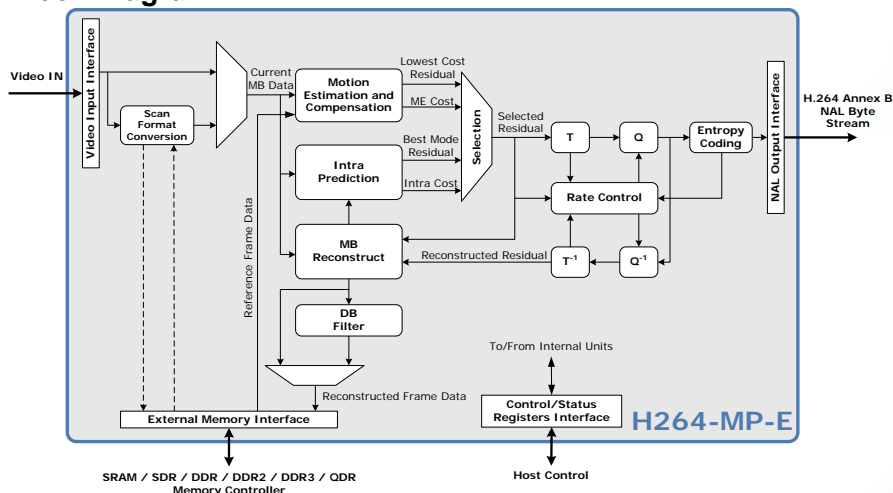
The core can encode at Full HD (1080p@30) or higher rates, even in low-cost FPGAs. Employing innovative techniques and algorithms, it provides video quality beyond typical H.264 hardware main profile encoders. The core can perform constant bit rate (CBR) compression that produces the highest possible quality while fitting the output to a specified bit rate, or constant-Qp, variable bit rate (VBR) compression to achieve a uniform quality level among frames.

The H.264-MP-E core can be configured to operate on Intra-Only mode, offering compression efficiency superior than this of JPEG and competitive to this of JPEG2000. Under this configuration the requirements for an external memory can be eliminated, the core's size is cut to half, and the output stream remains H264 compliant. With Intra-only compression each frame is coded independently, allowing for smaller processing delays, easier video editing, and enhanced error resilience.

The core is designed for ease and trouble-free integration. It can automatically convert incoming frames to the macroblock format required by the H.264 standard, and it outputs the standard H.264 Annex B NAL byte stream. Also, the employed CBR algorithm provides user-controlled granularity, and the CBR output stream is HRD compliant respecting decoder's buffering requirements. Furthermore, the core operates independently from a host processor and is run-time programmable for user control over compression parameters and bit rate options. Finally, a flexible external memory interface makes the core independent of memory type—supporting SRAM, SDRAM, or DDRAM—and more tolerant to the large delays and latencies typically present on a shared bus architecture.

The H.264-MP-E core is designed for reuse and reliability, and has been rigorously verified and FPGA proven. System integration is facilitated by the core's complete verification environment, with additional aids for system-on-chip simulation available such as a software bit-accurate model and a complete hardware/software reference design system.

Block Diagram



System Integration

- Processor-independent, stand-alone operation
- Independent of external memory type (DDR2/3, SDRAM, SRAM, etc.)
- Glue-less connection to CAST memory controllers
- Low latency
- Bit Accurate Model
- Available Application Platform hardware/software package

Applications

The H264-MP-E core efficiently handles extended definition (ED) through high definition (HD) video, and is suitable for a range of applications including surveillance and monitoring, video conferencing, and streaming video on demand.

Functional Description

The H264-MP-E core is a hardware implementation of the H.264 main video compression algorithm designed to process video with resolution up to 4kx4k pixels. It consists of a number of functional blocks, as shown in the diagram and de-scribed here.

The core accepts sequentially the 8-bit samples of the 4:2:0 YUV input video through the Video Input Interface. It converts the supported planar and interleaved input video scan formats to the H.264 native macroblock scan order via the Scan Format Conversion block.

For each block of pixels, the Intra Prediction unit generates a suitable prediction. In the case of P-frames, the Motion Estimation and Compensation Unit also generates a prediction, operating with quarter-pixel accuracy. The prediction cost of each unit is estimated using Lagrange multipliers, and the best is selected for encoding.

The residual information is calculated from the difference between the current block and the prediction. Constant or variable bit rate calculations are applied. The data is then transformed and quantized to be encoded by the Entropy Coding unit.

The transformed, quantized residual is also used to reconstruct a reference frame, which will be used during the encoding of future P-frames. This is achieved by inverse quantization and transformation of the residual, which is then added back to the prediction. Finally, the reconstructed frame is filtered before being stored back in the external memory.

The core can perform macroblock skipping that is important for low data rate applications, and supports multiple slices that enhance error resilience of the compressed stream.

Implementation Results

H264-MP-E reference designs have been evaluated in a variety of technologies. The following are ASIC, pre-layout, results for H264-MP-E core, reported from synthesis tool and silicon vendor design kit under worst case conditions. Internal memory figures are given for video sequences with resolution up to 1920x1080.

ASIC Technology	Eq. NAND2 gates	Fmax (MHz)	Throughput (MPixels/s)	Memory (kbits)
TSMC 130nm	690 K	275	112	725
TSMC 90nm	600 K	333	136	725

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL (VHDL or Verilog-2001) RTL source code.
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Synthesis scripts.
- Simulation script, vectors and expected results.
- Software (C++) Bit-Accurate Model and test-vector generator
- Comprehensive user documentation, including detailed specifications and a system integration guide.

Evaluation

The video encoder's extremely high visual quality is best evaluated by compressing examples of an application's actual input video. There are three ways to do this.

- Work directly with CAST's video compression engineers,
- Use the available BAM for software simulation, or
- Use the available H264-AP H.264 Application Platform, a board and software package combining the H.264 Encoder, memory and controller, and other IP cores with software drivers and a graphical user interface for H.264 control.

Please contact CAST Sales to discuss your specific project requirements (sales@cast-inc.com) (+1 201.391.8300).