



# H264-LD-BP

## Low-Power AVC/H.264 Baseline Profile Decoder

The H264-LD-BP IP core implements a silicon and energy efficient hardware video decoder able to process H.264 streams produced by the H264-E-BPS, H264-E-BPF and H264-E-BIS video encoder cores available from CAST.

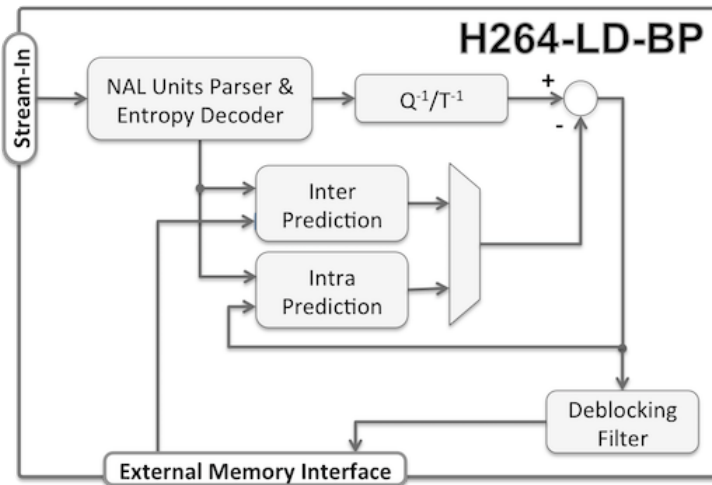
The H264-LD-BP is extremely small, requiring 6K LUTs and 11.5 BRAMs. Its small silicon footprint, low bandwidth requirements, and zero software overhead enable extremely cost-effective and low-power FPGA implementations.

The H264-LD-BP is designed for straightforward, trouble-free integration. It operates on a stand-alone basis such that decoding proceeds without any assistance or input from the host processor. The decoder's memory interface—used to store reconstructed video data—is extremely flexible: it operates on a separate clock domain, is independent from the external memory type and memory controller, and is tolerant to large latencies. The decoder reports decompressed video parameters, detects and reports bit stream errors to the system, and simplifies video cropping at its output. The core is optionally delivered with a raster-to-block converter, and wrappers for AMBA® AHB, AXI, or AXI-Streaming buses are available.

Customers can further decrease their time to market by using CAST's integration services to receive complete video encoding/decoding subsystems. These integrate the decoder core with video encoders, video and networking interface controllers, networking stacks, or other CAST or third-party IP cores.

The H264-LD-BP IP core is designed using with industry best practices and has been multiple times production proven. Its deliverables include a complete verification environment and a bit-accurate software model.

### Block Diagram



### Features

Low-power AVC/H.264 decoder, with small silicon footprint and optimized for low-latency, low-bit-rate video streaming

- Decodes streams produced by the H264-E-BPS, H264-E-BPF, and H264-E-BIS cores

#### Video Formats

- Progressive or Interlaced, 4:2:0 YCbCr with 8 bits per color sample
- Single-channel SD, ED, and Full-HD capable even in low-cost FPGAs
- Optional multichannel decoding

#### Small and Low-Power

- 6k LUTs & 11.5 BRAMs
- Less than half the typical silicon footprint and small external memory bandwidth mean it uses less power than competitive hardware H.264 decoders
- Consumes much less power than any equivalent software or software-hardware decoder

#### Ease of Integration

- Zero CPU overhead, stand-alone operation
- Flexible external memory interface. Uses separate clock, is independent of memory type and tolerant to latencies
- AMBA® Interface Options: DMA-capable AMBA® AHB, AXI or AXI-Streaming

#### Supported Coding Tools

- I and P Slices
- Single Reference Frame
- Motion vector up to – 32.00/+ 31.75 pixels down to ¼ pel accuracy
- All intra16x16 and most intra 4x4 modes
- Multiple slices per frame
- Block skipping
- Deblocking filter

## Silicon Resources Utilization

The H264-LD-BP can be mapped to any Xilinx Family (provided sufficient silicon resources are available) and optimized to suit the particular project's requirements. The following table provides sample resource utilization data for different Xilinx Device Families.

	LUTs	BRAMs	DSPs
KINTEX ULTRASCALE	6k	11.5	0
KINTEX-7	6k	11.5	0
ARTIX-7	6k	11.5	0

Multiple H264-LD-BP cores can be combined to decode streams produced by the H264-E-BPF core. The following table indicates the number of H264-LD-BP cores that would be required for different video formats in different Xilinx families.

	720p30	720p60	1080p30	1080p60
KINTEX ULTRASCALE	✓(1)	✓(1)	✓(2)	✓(3)
KINTEX-7	✓(1)	✓(2)	✓(2)	✓(3)
ARTIX-7	✓(1)	✓(2)	✓(3)	✓(4)

Note: List of video formats is not exhaustive.

## Evaluation

Potential customers can readily evaluate the video decoder's low latency characteristics by using the [Video over IP](#) reference design with compressed stream captured over Ethernet, and decoded video driving an HDMI interface.

## Deliverables

The core includes everything required for successful implementation:

- Post-synthesis EDIF (netlist licenses)
- Sophisticated self-checking Testbench
- Synthesis scripts.
- Simulation script, vectors and expected results.
- Comprehensive user documentation.

## Related Cores

The H264-LD-BP is one member of the family of H.264 encoder & decoder cores that CAST offers that includes the following members:

- [H264-E-BPS](#): Low Power Baseline Profile Encoder
- [H264-E-MPS](#): Low Power Main Profile Encoder
- [H264-E-HIS](#): Intra-Only High Profile Encoder
- [H264-E-BPF](#): Ultra-Fast Baseline Profile Encoder
- [H264-D-BP](#): Baseline Profile Decoder

Please visit [www.cast-inc.com](http://www.cast-inc.com) to learn more