H264-HP-E
H.264/AVC High Profile Video Encoder Core

Implements a hardware H.264 video encoder that supports the ISO/IEC 14496-10/ITU-T H.264 High Profile specification.

The High Profile H.264 Encoder Core supports real-time encoding of 4:2:0 and 4:2:2 video streams, up to Level 5.2, in 8-, 10-, or 12-bit sample depths. An Intra-only encoder variation features extremely low, sub-frame latency, can operate without an external memory, requires half the silicon resources, and is suitable for AVC-Intra 50 and AVC-Intra 100 encoder implementations.

The core provides great quality for all types of video and transmission bit rates. Under Constant Bit Rate mode (CBR), it preserves uniform quality while respecting the bit rate—even for the most challenging video content—by making multiple quantization adjustments within a single frame and by selecting the encoding mode based on run-time adaptive models. This allows the core to rapidly adapt to inter- and intra-frame video content variations and the output stream to comply with the hypothetical reference decoder’s coded-picture buffer (HRD-CPB) requirements of the H.264 spec, ensuring uninterrupted video decoding.

The encoder is designed for easy integration. It operates independently of the system processor and features simple interfaces that make system integration straightforward. Furthermore, the core works with any type of external memory and memory controller devices via a flexible external memory interface. Best-practice RTL coding and high-quality deliverables, tested and proven in dozens of designs, ensure that no bad surprises will arise from verification through FPGA or ASIC technology mapping.

Applications
The H264-HP-E produces exceptional video quality and features an advanced rate control that makes it ideal for broadcasting, high-end professional cameras, video storage, and other demanding high-definition video applications.

Block Diagram

Features
Supported H.264 Profiles
- High 10, High 4:2:2, High 4:4:4 (12 bit 4:2:2 or 4:2:0)
- Main and Constrained-Baseline
- Intra versions of all the above

Supported Video Formats
- 4:2:0 and 4:2:2 YCbCr input with 8, 10 and 12 bits per color sample
- Annex B NAL byte stream output
  - Constant Bit Rate (CBR) or variable bit rate Constant Quality (CQP) modes

High Performance
- Level up to 5.2,
  - Up to 240 Mbits/s for CAVLC
  - Up to 135 Mbits/s for CABAC
- High throughput
  - 2.5 clocks/pixel for 4:2:0
  - 2.75 clocks/pixel for 4:2:2

Advanced Rate Control
- Rate control operates on sub-frame basis, uses micro-adjustments per MB, and employs run-time adaptive models
  - Optimizes rate distortion and perceived video quality
  - Respects decoder buffer: HRD CPB compliant CBR output
  - Provides uniform quality and rapidly adopts to temporal and spatial video variations
- Allows for end-to-end latency
- Ultra-low sub-frame latency with optional Intra-Refresh

Ease of Integration
- CPU-less, stand-alone operation
- No need for external raster conversion
  - Support for planar, interleaved and macroblock input scan
- Flexible external memory interface
  - Independent of memory type
  - Low bandwidth requirements and tolerant to latencies, for shared memory architectures
- Flexible video input and stream output interfaces
  - Flow-controllable, streaming-capable Avalon-ST interfaces
  - Optional wrappers for AMBA® AHB or AXI SoC bus
- Run-time tunable operation and on-the-fly target rate changes
Features Continued

Encoding Tools
- CABAC or CAVLC Encoding
- Motion Estimation
  - Optimal, Full-Search
  - 32x20 or higher search area; down to 1/8 pel accuracy
  - Variable block size; up to four motion vectors per MB
- Sophisticated block skipping for fewer motion artifacts in low bit rates
- All 16x16 and 4x4 luma, and all chroma intra prediction modes
- In-Loop deblocking filter
- Multiple slices for error resilience
- Optional thresholding of quantized transform coefficients

Performance and Resources Utilization

<table>
<thead>
<tr>
<th>H264-HP-E Configuration</th>
<th>Performance</th>
<th>Area (Slices)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Artix-7</td>
<td>Kintex-7</td>
</tr>
<tr>
<td>IDR 8-bit 4:2:2</td>
<td>1080p24‡</td>
<td>1080p30</td>
</tr>
<tr>
<td>IDR, P 8-bit 4:2:2</td>
<td>1080p24‡</td>
<td>1080p30</td>
</tr>
<tr>
<td>IDR 10-bit 4:2:2</td>
<td>1080p24‡</td>
<td>1080p30</td>
</tr>
<tr>
<td>IDR, P 10-bit 4:2:2</td>
<td>1080p24‡</td>
<td>1080p30</td>
</tr>
</tbody>
</table>

1: -1 speed grade or faster  2: -2 speed grade or faster
‡: Exact resource requirements depend on target device and core configuration

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:
- Post-synthesis EDIF or NGC netlist
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Synthesis scripts
- Simulation script, vectors and expected results
- Software (C++) Bit-Accurate Model and test-vector generator
- Comprehensive user documentation, including detailed specifications and a system integration guide

Evaluation

The video encoder’s extremely high visual quality is best evaluated by compressing examples of an application’s actual input video. There are three ways to do this:
- Work directly with CAST’s video compression engineers,
- Use the available BAM for software simulation, or
- Use the available H264-AP H.264 Application Platform. This board and software package combines the Encoder, memory and controller, and other cores with software drivers and a graphical user interface for H.264 control.

Please contact CAST Sales to discuss your specific project requirements: sales@cast-inc.com, +1 201.391.8300.

H.264 Encoders Family

A family of H.264 encoder cores is available from CAST. The following table outlines the family members and their basic features.

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>Slice type(s)</td>
<td>IDR, P</td>
<td>IDR</td>
<td>Main</td>
<td>Main</td>
<td>High 10, High 4:4:4</td>
<td>High 10 Intra, High 4:4:4 Intra</td>
</tr>
<tr>
<td>Chroma format(s)</td>
<td>4:2:0</td>
<td>4:2:0</td>
<td>4:2:0</td>
<td>4:2:0</td>
<td>4:2:0</td>
<td>4:2:0</td>
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<tr>
<td>Sample depth (bits)</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8, 10, 12</td>
<td>8, 10, 12</td>
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<tr>
<td>CAVL / CABAC</td>
<td>/</td>
<td>/</td>
<td>/</td>
<td>/</td>
<td>/</td>
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</tr>
<tr>
<td>Rate control (CBR &amp; CQP-VBR) with separate Luma / Chroma QP control</td>
<td>/</td>
<td>/</td>
<td>/</td>
<td>/</td>
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<tr>
<td>AVC-Intra 50 / 100 / Ultra suitability</td>
<td>X</td>
<td>X</td>
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<tr>
<td>Throughput (clocks/pixel)</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5 - 2.75</td>
<td>2.5 - 2.75</td>
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<tr>
<td>Sub-frame latency capable</td>
<td>X</td>
<td>X</td>
<td>X</td>
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</table>

Note 1: 4:4:4 profiles support 12bits for 4:2:0 or 4:2:2

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