

CAST

CMMI-H264-E AHB Multimedia Interface for H.264-E Encoder Core

The CAST Multimedia Interface IP core (CMMI) implements a simple interface between an AMBA™ AHB bus and the CAST H264-E H.264/AVS Video Encoder Core.

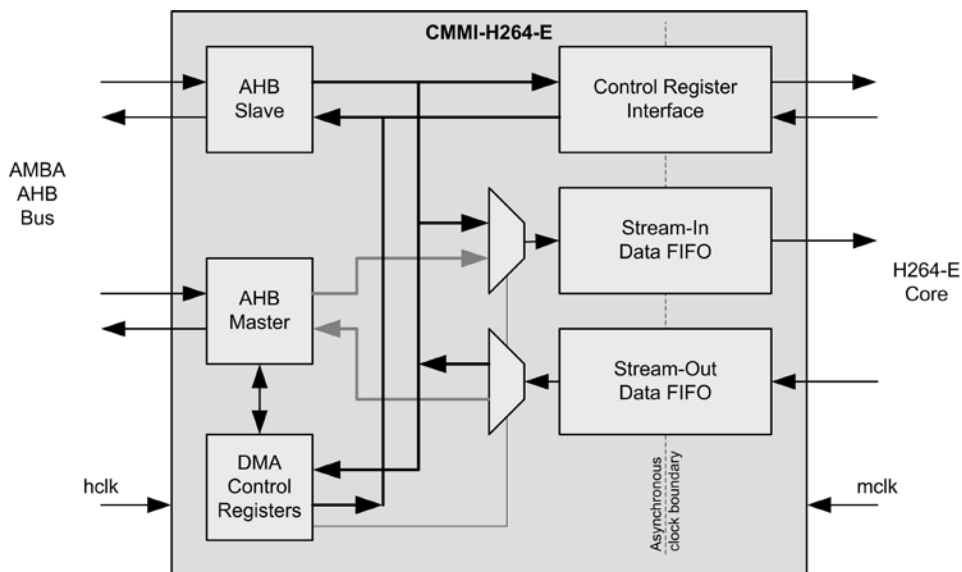
The CMMI integrates data paths for core control register access, stream data transfer in both directions, and a dual-channel DMA controller. It allows removing stream-in or stream-out data paths. DMA channels can be removed from the implementation using the core parameters. This allows reducing the size and memory requirements of the CMMI core in applications where the stream-in data input of the H.264 encoder core is directly coupled with a sensor.

Applications

This Multimedia Interface core is suitable for H.264 Encoder core integration in a wide range of applications, such as:

- Surveillance and monitoring
- Video conferencing
- Video on demand
- Other SD and HD Video applications

Block Diagram



Features

- AMBA™ AHB bus specification rev. 2.0 compliant
- Easy system integration with H.264 Encoder Core
- Independent video-in and stream-out FIFOs
- Configurable FIFO size
- FIFO status register
- Two-channel DMA controller
- FIFO data accessible both from SoC bus and by DMA controller
- Burst transfer optimization for slave and DMA transfers
- Interrupt-on-finished transfer for both slave and DMA transfers
- Adjustable AHB bus access timeout to stream FIFOs
- Asynchronous clock domain boundary
- Possible to remove video-in or video-out stream data path
- Optional support of other SoC buses
- Reference System Design with PCI Express and H264-E cores available

Functional Description

The core is divided into five modules:

AHB Slave takes care of data transfers when accessed from the AHB bus.

AHB Master initiates data transfers on the AHB bus when directed by the DMA.

Control Register Interface implements an asynchronous clock boundary and backend register bus control.

DMA Control Registers contain a set of DMA control/status registers.

Stream-In Data FIFO buffers data processed by a multimedia core for further AHB bus transfer. It also implements an asynchronous clock boundary.

Implementation Results

CMMI reference designs have been evaluated in a variety of technologies; the results from several implementations of the core are shown below.

Configuration	Technology	Approx. Area
CMMI without DMA	TSMC 0.09 μm	11,471 gates
CMMI without DMA	TSMC 0.13 μm	13,130 gates
CMMI without DMA	TSMC 0.18 μm	13,885 gates
CMMI with 2CH DMA	TSMC 0.09 μm	15,790 gates
CMMI with 2CH DMA	TSMC 0.13 μm	17,905 gates
CMMI with 2CH DMA	TSMC 0.18 μm	19,044 gates

Example Application

The CMMI has been implemented in an FPGA-based Reference System Design that integrates a number of CAST cores in a working demonstration platform.

The system includes the H264-E and CMMI-H264-E AHB Interface, CPXP-EP PCI Express, and DDR2-SDRAM-CTRL Memory Controller cores, plus associated software.

The encoder receives raster-scan video data via the PCI Express bus. It encodes the video to H.264 format, then sends the data via the PCI Express bus to a PC for further processing. The CMMI core works as an interfacing module between the H.264 core and PCI Express cores over the AMBA AHB bus.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation. It has also been verified in a prototyping FPGA board platform.

Deliverables

The core is available in ASIC (synthesizable) or FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source
- Sophisticated HDL Testbench including models of interfaces, and the core
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script
- Comprehensive user documentation

