H264-E-MPS
Low-Power AVC/H.264 Main Profile Encoder

The H264-E-MPS IP core is a video encoder supporting the Main Profile of the ISO/IEC 14496-10/ITU-T H.264 standard. It Implements an energy-efficient hardware encoder that is optimized for ultra-low-latency video streaming at low bit rates.

The H264-E-MPS encoder requires less than half the silicon area of most competing hardware encoders—under 250K gates—allowing for very cost-effective ASIC or FPGA implementations. Its small silicon footprint, low external memory bandwidth requirements, and zero software overhead enable H.264 coding at an extremely low energy cost.

Despite being small, the H264-E-MPS produces high quality video, especially at low bit-rates, and is suitable for systems with low latency requirements. It uses constant quantization to output video streams of Variable Bit Rate (VBR), or automatically regulates quantization multiple times within a frame to output Constant Bit Rate (CBR) streams.
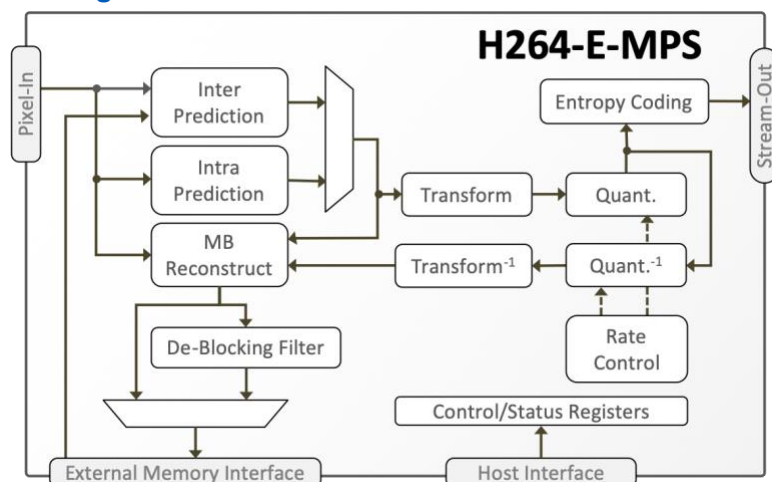
In CBR mode it responds rapidly to temporal or spatial changes in the video content. This can be combined with an artifacts-free Intra-Refresh coding implementation to effectively eliminate bit-rate peaks, while preserving the periodic intra-coded references. As a result, the stream buffers can be smaller than those typically required, and the end-to-end latency can be brought down to frame or sub-frame levels. Video quality at low bit rates is preserved, as the encoder intelligently uses block-skipping and quantization coefficient thresholding to reduce bit rate at minimal quality loss, and uses the in-loop deblocking filter to eliminate the blocking artifact.

The core was designed for ease of use and integration. Once initially programmed, it operates without any assistance from the host processor. The encoder's memory interface is extremely flexible: it operates on a separate clock domain, is independent from the external memory type and memory controller, and is tolerant to large latencies. The core is optionally delivered with a raster-to-block converter, and wrappers for AMBA® AHB, AXI, or AXI-Streaming buses are available.

Customers can further decrease their time to market by using CAST's integration services to receive complete video encoding subsystems. These integrate the encoder core with video and networking interface controllers, networking stacks, or other CAST or third-party IP cores.

The H264-E-MPS IP core is designed using industry best practices. Its deliverables include a complete verification environment and a bit-accurate software model.

Block Diagram

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Coding Tools

- Variable Bit Rate with Constant Qp (VBR-CQP) and Constant Bit Rate (CBR)
- CAVLC or CABAC Entropy Encoding
- Efficient Inter- and Intra-Prediction
  - Motion vector up to –16.00/+15.75 pixels down to ¼ pel accuracy
  - All intra 16x16 and most intra 4x4 modes
- Options for improved error resilience
  - Multiple slices per frame
  - Intra-only coding
- Options for better quality at low bit-rates
  - Block skipping
  - Deblocking filter
  - Separate quantization values for luma and chrome
  - Thresholding of quantized transform coefficient

Silicon Resources Utilization

The H264-E-MPS synthesizes to less than 250k gates and requires 150 Kbits of internal memory.

Deliverables

The core is available in source-code HDL (Verilog or VHDL) or as a targeted netlist, and its deliverables include everything required for successful implementation.:

- Sophisticated self-checking Testbench
- Synthesis scripts.
- Simulation script, vectors and expected results.
- Software (C++) Bit-Accurate Model and test-vector generator
- Comprehensive user documentation.

Evaluation

Potential customers can readily evaluate the video encoder's compression efficiency by using:

- Available sample compressed video streams
- The available Bit-Accurate Model with your choice of input videos
- The Video over IP reference design with video captured over an HDMI interface

Please contact CAST to arrange for your evaluation preference.

H.264 Cores Family

The H264-E-MPS is one member of the family of H.264 cores that CAST offers. The following table summarizes the family's encoders and highlights the cores' basic features. H.264 decoders are also available, the baseline H256-D-BP and low-power LD-BP.

H.264 ENCODER CORES	H264-E-BIS Intra-Only Baseline Profile	H264-E-BPS Low-Power Baseline Profile	H264-E-MPS Low-Power Main Profile	H264-E-CFS Ultra-Low-Power Baseline Profile	H264-E-HIS Intra-Only High Profile	H264-E-BPF Ultra-Fast Baseline Profile
Cycles/Pixel	4	4	4	4	2.5	2 or 1
Silicon Resources *	Very Small	Small	Small	Small	Moderate	Moderate-High
Profile	Constrained Baseline	Constrained Baseline	Main	Constrained Baseline	High 10 Intra	Constrained Baseline
Slices Types	IDR	IDR, P	IDR, P	IDR, P	IDR	IDR, P
Chroma Formats	4:2:0	4:2:0	4:2:0	4:2:0	4:2:0	4:2:0
Bits per sample	8	8	8	8	8, 10	8
Progressive/Interlaced	✔ / ✔	✔ / ✔	✔ / ✘	✔ / ✘	✔ / ✘	✔ / ✔
Multiple video channels	Optional	Optional	Optional	Optional	✘	Optional
CAVLC / CABAC	✔ / ✘	✔ / ✘	✘ / ✔	✔ / ✘	✔ / ✘	✔ / ✘
CBR and VBR	✔	✔	✔	✔	✘	✔
Intra-Refresh	N/A	✔	✔	✔	N/A	✔
Multiple Slices	✔	✔	✔	✔	✘	✔
Compressed Frame Store	✘	✘	✘	✔	N/A	N/A

* Very Small <100k Gates, Small < 200k Gates, Moderate < 500K Gates, and High > 500KGates