H264-D
H.264 Video Decoder Core

Implements a hardware video decoder compatible with the Constrained Baseline Profile, Main Profile, or High 4:2:2 Profile of the H.264/AVC standard (also known as MPEG-4 Part 10).

The core can decode streams at the 5.1 level of the standard, which includes 4k, 4,096×2,048 video at 30 fps encoded at 240Mbits/second. An optional High 4:2:2 Profile capability supports decoding streams at rates up to 300 MBits/second.

The video decoder is designed for straightforward, trouble-free SoC integration. It operates on a stand-alone basis such that decoding proceeds without any assistance or input from the host processor. A standard AMBA® APB system bus interface gives the host real-time control and status access. A flexible memory interface for reading the incoming compressed video and storing the resulting decompressed video is independent of memory type—supporting SRAM, SDRAM, or DDRAM—and tolerant to the large delays and latencies typically present on a shared bus architecture. Furthermore, the core's decoded image storage can be configured to match the input video stream, allowing the minimum amount of memory to be allocated for each specific stream.

The core is designed for reuse and reliability, and has been rigorously verified and FPGA proven. A complete ‘C’ reference driver and fully documented API facilitate system integration. An available FPGA-based reference system using the core provides a complete development environment for evaluation and early software development.

Applications
The decoder core's support for multiple H.264 profiles and high-resolution, 4.1 level video makes it an excellent choice for a variety of applications, including:

- Satellite TV/IPTV/Cable Set-top boxes
- Blu-ray DVD players
- Video capable portable devices
- Surveillance systems
- Video conferencing
- Video game consoles

Block Diagram

Features

H.264 Video Decoding
- Supports the H.264/AVC standard (also known as MPEG-4 Part 10).
  - Main Profile
  - Constrained Baseline Profile
  - High422 Profile (Optional)
  - Level up to 5.1 (4k, 4,096×2,048 video at 30 fps encoded at 240Mbits/second)

Main Profile Support
- I, P, and B-Slices
- CAVLC and CABAC
- In-loop Deblocking Filter
- Multiple reference frames
- Interlaced Coding
- No limitations on motion-vectors range or number per macroblock

High 4:2:2 Profile Support
- Transform Adaptivity
- Quantization Scaling Matrices
- Separate Cb/Cr Qp Control
- 4:2:2, 4:2:0 and 4:0:0 (monochrome) Video Format

Easy SoC Integration
- Processor-independent, stand-alone operation
- Independent of external memory type: can use DDR2/3, SDRAM, SRAM, and others
- Tolerant to memory latency
- Includes ‘C’ reference driver and fully-documented API
- Available ready-to-run FPGA Development and Evaluation Platform integrates decoder core with peripherals, memory, interfaces, and essential software
Implementation Results

The H264-D core was developed using best-in-class design principles and is very efficient in resource usage and clock rates. On a typical 65nm technology, the core synthesizes to about 380k eq, gates and uses 300kbits of internal RAM. Please contact CAST for detailed area and timing results for any specific technology you require.

FPGA Development & Evaluation Platform

The Development & Evaluation Platform available with this core is implemented in an FPGA and allows quick and cost-effective evaluation and early software prototyping.

The ready-to-run platform includes a 32-bit host processor capable of running custom applications, DVI and other built-in interfaces, and a peripherals suite running a flash-based ROM monitor that loads at power-up.

The ROM monitor allows for the development and download of customer specific application code developed using GCC, enabling simultaneous hardware and software evaluation.

Support

The core as delivered is warranted against defects for 90 days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The H264-D has been rigorously verified using random and directed testing covering corner condition across a wide variety of resolutions. Furthermore, it has been validated using external and internal compliance test suites. The results of the compliance testing are available upon request. Extensive interoperability testing has also been conducted using a wide variety of shipping encoder products.

Deliverables

The core includes everything required for successful implementation:

- HDL RTL source code (soft core) or a post-synthesis EDIF netlist (firm core)
- Reference driver, API and video player application in C
- Sophisticated shelf-checking HDL Testbench
- Simulation script, vectors, expected results, and timing constraints simulation summary
- Synthesis (soft) or place and route (firm) script
- Comprehensive user documentation, including a fully documented API, and functional specification.