H264-D-BP

Low-Latency AVC/H.264 Baseline Profile Decoder

The H264-D-BP IP core is a video decoder complying with the Constrained Baseline Profile of the ISO/IEC 14496-10/ITU-T H.264 standard. It implements a hardware decoder with very low latency and high throughput that is suitable for live streaming and other delay-sensitive applications up to full HD resolution.

The decoder adds just one macroblock line of latency, which means a negligible real-world latency under one msec for most widely used video formats, including HD/720p and Full-HD/1080p video.

The H264-D-BP is designed for straightforward, trouble-free SoC integration. It operates on a stand-alone basis such that decoding proceeds with no assistance or input from the host processor. The decoder's memory interface—used to store reconstructed video data—is independent from the external memory type and memory controller, and is tolerant to large latencies. Optionally, the core can be reduced to support only Intra-coded streams, in which case the required external memory is just 128kB and can be implemented on-chip. The decoder reports decompressed video parameters, detects and reports bit stream errors to the system, and simplifies video cropping at its output. The core is optionally delivered with a raster-to-block converter, and wrappers for AMBA® AHB, AXI, or AXI-Streaming buses are available.

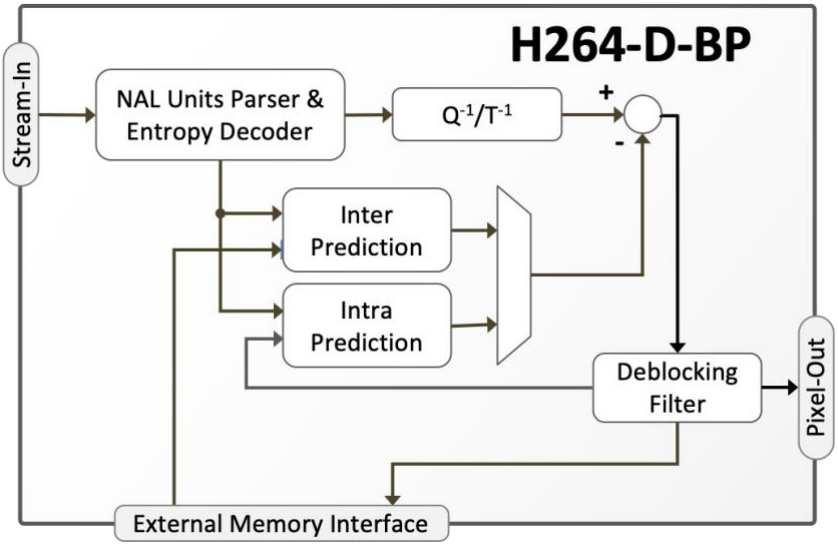
Customers can further decrease their time to market by using CAST's integration services to receive complete video encoding/decoding subsystems. These integrate the decoder core with video encoders, video and networking interface controllers, networking stacks, or other CAST or third-party IP cores.

The H264-D-BP IP core has been verified with Fraunhofer's compliance test stream suit, and has been silicon and production proven. Its deliverables include a complete verification environment and a bit-accurate software model.

Applications

The H264-D-BP is suitable for broadcasting, surveillance, industrial, defense, and medical live-streaming applications, with low-latency requirements and resolutions up to Full-HD.

Block Diagram



FEATURES

Constrained Baseline Profile AVC/H.264 decoder

- Ultra-Low-Latency: less than one msec latency for most widely used formats
- High performance: 2.5 cycles per pixel; Full-HD capable

Standard Support

- ISO/IEC 14496-10/ITU-T H.264, Constrained Baseline Profile specification
  - I and P slices (Intra-only version also available)
  - Multiple slices per frame
  - Multiple reference frames
  - Multiple sequence parameter sets (SPS)
  - Multiple picture parameter sets (PPS)
  - In-loop deblocking filter
  - CAVLC entropy decoding
- Real time performance up to level 4.1

Video Formats

- Progressive, 4:2:0 YCbCr with 8 bits per color sample
- From QCIF (176x144), to 2048x2048 resolutions

Low Latency

- No decoded frame buffering
- Decoded pixels are streamed out with less than one macro-block line of latency
- Less than 1 msec for almost all widely used video formats

Ease of Integration

- Zero CPU overhead, stand-alone operation
- AMBA® AXI external memory interface is independent of memory type and tolerant to latencies
- Streaming interfaces for bit-stream and pixel data with flow control; easily bridged to AMBA® AXI Streaming
- Error catching and reporting capability
- Reports video format and enables cropping
- Optional Block to Raster Conversion

Maturity

- Silicon proven
- Verified with Fraunhofer H.264 Compliance Test Streams Suite

Silicon Resources Utilization

The H264-D-BP can be mapped to any Intel FPGA (provided sufficient silicon resources are available). The following table provides sample performance and resource utilization data for different Intel Device Families.

	720p30	720p50	720p60	1080p30
StratixV	✓	✓	✓	✓
Arria10	✓	✓	✓	v
CycloneV	✓	×	×	×
ALMs	32K			
Memory bits	532k			
DSPs	19			

1: List of video formats is not exhaustive. Indicated video formats may not be supported at devices of all speed grades

An Intra-only version of the core (i.e. decoder core limited to decoded I-frames only) occupies about 20% less silicon resources, and requires just 128kB of external memory

Evaluation

Potential customers can readily evaluate the video decoder's low latency characteristics by using the Video over IP reference design with the compressed stream captured over Ethernet, and the decoded video driving an HDMI interface.

Deliverables

The core is available in source-code VHDL or as a targeted netlist, and its deliverables include everything required for successful implementation:

- Sophisticated self-checking Testbench
- Synthesis scripts.
- Simulation script, vectors and expected results.
- Software Bit-Accurate Model
- Comprehensive user documentation.

H.264 Cores Family

The H265-MP-D is one member of the family of H.264 cores that CAST offers. The following tables summarize the family's encoders and decoders and highlight the cores' basic features.

H.264 Encoder Cores	**H264-E-BIS** Intra-Only Baseline Profile	**H264-E-BPS** Low-Power Baseline Profile	**H264-E-MPS** Low-Power Main Profile	**H264-E-CFS** Ultra-Low-Power Baseline Profile	**H264-E-HIS** Intra-Only High Profile	**H264-E-BPF** Ultra-Fast Baseline Profile
Cycles/Pixel	4	4	4	4	2.5	2 or 1
Silicon Resources *	Very Small	Small	Small	Small	Moderate	Moderate-High
Profile	Constrained Baseline	Constrained Baseline	Main	Constrained Baseline	High 10 Intra	Constrained Baseline
Slices Types	IDR	IDR, P	IDR, P	IDR, P	IDR	IDR, P
Chroma Formats	4:2:0	4:2:0	4:2:0	4:2:0	4:2:0	4:2:0
Bits per sample	8	8	8	8	8, 10	8
Progressive/Interlaced	✓ / ✓	✓ / ✓	✓ / ×	✓ / ×	✓ / ×	✓ / ✓
Multiple video channels	Optional	Optional	Optional	Optional	×	Optional
CAVLC / CABAC	✓ / ×	✓ / ×	× / ✓	✓ / ×	✓ / ×	✓ / ×
CBR and VBR	✓	✓	✓	✓	×	✓
Intra-Refresh	N/A	✓	✓	✓	N/A	✓
Multiple Slices	✓	✓	✓	✓	×	✓
Compressed Frame Store	×	×	×	✓	N/A	N/A

* Very Small <100k Gates, Small < 200k Gates, Moderate < 500K Gates, and High > 500KGates

H.264 Decoder Cores	**H264-D-BP** Low Latency Baseline Profile Decoder	**H264-LD-BP** Low Power Baseline Profile Decoder
Profile	Constrained Baseline	Constrained Baseline
Profile Compatibility	Full	Limited to streams from the H264-E-BPS/BPF, BIS cores
Additional Features	×	Interlaced with Main Profile Syntax
Throughput (cycles/pixel)	2.5	4
Silicon Resources	Moderate	Small

* Very Small <100k Gates, Moderate < 500K Gates