H264-BP-E
H.264/MPEG-4 AVC HD & ED Video Encoder Core

Implements a hardware H.264 video encoder that supports the ISO/IEC 14496-10/ITU-T H.264 Constrained Baseline Profile specification.

The Baseline Profile H.264 Encoder Core supports real-time encoding of 4:2:0 video with 8-bits per color sample, and provides performance up to Level 5.2. An Intra-only encoder variation features extremely low, sub-frame latency, can operate without an external memory and requires half the silicon resources.

The core provides great quality for all types of video and transmission bit rates. Under Constant Bit Rate mode (CBR), it preserves uniform quality while respecting the bit rate—even for the most challenging video content—by making multiple quantization adjustments within a single frame and by selecting the encoding mode based on runtime adaptive models. This allows the core to rapidly adapt to inter- and intra-frame video content variations and the output stream to comply with the hypothetical reference decoder’s coded-picture buffer (HRD-CPB) requirements of the H.264 spec, ensuring uninterrupted video decoding.

The encoder is designed for easy integration. It operates independently of the system processor and features simple interfaces that make system integration straightforward. Furthermore, the core works with any type of external memory and memory controller devices via a flexible external memory interface. Best-practice RTL coding and high-quality deliverables, tested and proven in dozens of designs, ensure that no bad surprises will arise from verification through FPGA or ASIC technology mapping.

Applications

The H264-BP-E core efficiently handles extended definition (ED) through high definition (HD) video, and is suitable for a range of applications including surveillance and monitoring, video conferencing, and streaming video on demand.

Block Diagram

Features

H.264 Video Encoding
- Fully compliant to the ISO/IEC 14496-10/ITU-T H.264 Constrained Baseline specification (MPEG-4 Part 10, Advanced Video Coding)

Supported Video Formats
- 4:2:0 YCbCr input with 8 bits per color sample
- Annex B NAL byte stream output
  - Constant Bit Rate (CBR) or variable bit rate Constant Quality (CQP) modes

High Performance
- Level up to 5.2 and Up to 240 MBits/s
- Only 2.5 clocks/pixel

Advanced Rate Control
- Rate control operates on sub-frame basis, uses micro-adjustments per MB, and employs run-time adaptive models
  - Optimizes rate distortion and perceived video quality
  - Respects decoder buffer: HRD CPB compliant CBR output
- Provides uniform quality and rapidly adapts to temporal and spatial video variations
- Allows for end-to-end latency
- Ultra-low sub-frame latency with optional Intra-Refresh

Ease of Integration
- CPU-less, stand-alone operation
- No need for external raster to Macro-Block conversion
  - Support for planar, interleaved and macroblock input scan
- Flexible external memory interface
  - Independent of memory type
  - Low bandwidth requirements and tolerant to latencies, for shared memory architectures
- Flexible video input and stream output interfaces
  - Flow-controllable, streaming-capable Avalon-ST interfaces
  - Optional wrappers for direct connection to an AMBA® AHB or AXI SoC bus
- Run-time tunable operation and on-the-fly target rate changes
Features Continued

Encoding Tools
- CAVLC Encoding
- Motion Estimation
  - Optimal, Full-Search
  - 32x20 or higher search area; down to ¼ pel accuracy
  - Variable block size; up to four motion vectors per MB
- Sophisticated block skipping for fewer motion artifacts in low bit rates
- All 16x16 and 4x4 luma, and all chroma intra prediction modes
- In-Loop deblocking filter
- Multiple slices for error resilience
- Optional thresholding of quantized transform coefficients

Performance and Resources Utilization

<table>
<thead>
<tr>
<th>H.264-BP-E Configuration</th>
<th>Performance</th>
<th>Area† (Slices)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDR 8-bit 4:2:0</td>
<td>720p60 1, 1080p30 2</td>
<td>8.5K - 9.5K</td>
</tr>
<tr>
<td>IDR, P 8-bit 4:2:0</td>
<td>720p60 2, 1080p30 3</td>
<td>15.5K - 17.5K</td>
</tr>
</tbody>
</table>

1 : -1 speed grade or faster  2 : -2 speed grade or faster  3 : -3 speed grade
† : Exact resource requirements depend on target device and core configuration

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:
- Post-synthesis EDIF or NGC netlist
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Software (C++) Bit-Accurate Model and test vector generator
- Simulation scripts, test vectors and expected results
- Place and route scripts
- Comprehensive user documentation, including detailed specifications and a system integration guide

Evaluation

The video encoder’s extremely high visual quality is best evaluated by compressing examples of an application’s actual input video. There are three ways to do this.
- Work directly with CAST’s video compression engineers,
- Use the available BAM for software simulation, or
- Use the available H264-AP H.264 Application Platform, a board and software package combining the H.264 Encoder, memory and controller, and other IP cores with software drivers and a graphical user interface for H.264 control.

Please contact CAST Sales to discuss your specific project requirements (sales@cast-inc.com) (+1 201.391.8300).

H.264 Encoders Family

A family of H.264 encoder cores is available from CAST. The following table outlines the family members and their basic features.

<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Profile</td>
<td>Constrained Baseline</td>
<td>Constrained Baseline</td>
<td>Main</td>
<td>Main</td>
<td>High 10, High 4:2:2, High 4:4:4† Predictive</td>
</tr>
<tr>
<td>Slice type(s)</td>
<td>IDR, P</td>
<td>IDR</td>
<td>IDR, P</td>
<td>IDR</td>
<td>IDR, P</td>
</tr>
<tr>
<td>Chroma format(s)</td>
<td>4:2:0</td>
<td>4:2:0</td>
<td>4:2:0</td>
<td>4:2:0</td>
<td>4:2:0, 4:2:2</td>
</tr>
<tr>
<td>Sample depth (bits)</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>10, 12</td>
</tr>
<tr>
<td>CAVLC / CABAC</td>
<td>✓</td>
<td>✓</td>
<td>✓ / ✓</td>
<td>✓ / ✓</td>
<td>✓ / ✓</td>
</tr>
<tr>
<td>Rate control (CBR &amp; CQP-VBR) with separate Luma / Chroma QP control</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>AVC-Intra 50 / 100 / Ultra suitability</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✓</td>
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<tr>
<td>Throughput (clocks/pixel)</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5 - 2.75</td>
</tr>
<tr>
<td>Sub-frame latency capable</td>
<td>✗</td>
<td>✓</td>
<td>✗</td>
<td>✓</td>
<td>✗</td>
</tr>
</tbody>
</table>

Note 1: 4:4:4 profiles support 12bits for 4:2:0 or 4:2:2.