The H16550S is a standard UART providing 100% software compatibility with the popular Texas Instruments 16550 device. It performs serial-to-parallel conversion on data originating from modems or other serial devices, and performs parallel-to-serial conversion on data from a CPU to these devices.

The H16550S can be run in either 16450-compatible character mode or in 16550-compatible FIFO mode, where an internal FIFO relieves the CPU of excessive software overhead.

Developed for easy reuse in FPGA or ASIC applications, the H16550S is available optimized for several technologies with competitive utilization and performance characteristics.

Applications

The H16550S can be utilized for a variety of serial communication applications including:

- Serial or modem computer interface
- Serial interface within modems and other devices

Features

- Capable of running all existing 16450 and 16550a software
- Fully Synchronous design. All inputs and outputs are based on rising edge of clock
- In FIFO mode, the transmitter and receiver are each buffered with 16 byte FIFOs to reduce the number of interrupts presented to the CPU
- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- Programmable baud generator divides any input clock by 1 to \((2^{16} - 1)\) and generates the 16 x clock
- Modem control functions (CTS\(_n\), RTS\(_n\), DSR\(_n\), DTR\(_n\), R\(_n\), and DCD\(_n\))
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8 bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1, 1½, or 2 stop bit generation
  - Baud generation
  - False start bit detection
  - Complete status register
  - Internal diagnostic capabilities: loopback controls for communications link fault isolation
  - Full prioritized interrupt system controls
Functional Description

The H16550S includes the following six major blocks. All the core’s inputs and outputs are fully synchronous to the rising edge of the CLK input.

**Interface**

Handles communication with the processor (or parallel) side of the system. Manages all writing and reading of internal registers.

**Registers**

Holds all of the device’s internal registers. Some information comes from the other blocks, but it is all gathered in the Registers block and made available to all blocks.

**RXBlock**

Handles the receiving of the incoming serial word. It is programmable to recognize data widths such as 5, 6, 7 or 8 bits, various parity settings, and different stop bits of 1, ½ and 2 bits. It checks for errors in the input data stream, and if the incoming word has no problems it is placed either in the Receiver Holding register or in the Receiver FIFO depending on the mode programmed.

**Interrupt Control**

Sends an interrupt signal back to the processor depending on the state of the FIFO and its received and transmitted data. Various levels of interrupt can be read from the Interrupt Identification register. Interrupts are sent in the condition of empty transmission or receiving buffers (or FIFOs), an error in the receiving of a character, or other conditions requiring the attention of the processor.

**Baud Rate Generator**

Takes the input clock, CLK, and divides it by a programmed value (from 1 to 2\(^{16} - 1\)). This divided clock is then divided by 16 to create the transmission clock called the Baudout clock.

**TXBlock**

Handles the transmission of data written to the Transmission Holding register (or transmit FIFO). It adds required start, parity and stop bits to the data being transmitted so that the receiving device can do the proper error handling and receiving.

**Component Substitution**

The H16550S megafuction is modeled after the Texas Instruments 16550, with the following differences. A wrapper is required to create a megafuction with the same functions; a sample wrapper is included.

- No provision is made for a crystal. The CLK input is designed to accept a standard digital input.
- The RCLK input in the Asynchronous version is replaced by CLK with rclk_enb which has the same frequency as BAUDOUTn.
- The bi-directional Data Bus has been split into an input and an output component. In order to use the megafunc-

Implementation Results

H16550S reference designs have been evaluated in a variety of technologies. The following are sample Altera results.

<table>
<thead>
<tr>
<th>Supported Family</th>
<th>Utilization</th>
<th>Fmax (MHz)</th>
<th>Quartus Version</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Family</td>
<td>LEs</td>
<td>Memory</td>
</tr>
<tr>
<td>Flex EPF10K30-1</td>
<td>749</td>
<td>3 EABs</td>
<td>69</td>
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<td>Acex EP1K30-1</td>
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<td>3 EABs</td>
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<tr>
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<td>2 M9Ks</td>
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<td>1 M4K / 1 M512</td>
<td>216</td>
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<tr>
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<td>1 M9K</td>
<td>125</td>
</tr>
</tbody>
</table>

Support

The megafuction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The megafuction has been verified through extensive simulation and rigorous code coverage measurements.
Deliverables

The megafuction is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Altera version includes:

- Post-synthesis EDIF netlist
- Wrapper for pin compatible replacement
- Sophisticated HDL Testbench (self-checking)
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide