

CAST



C8254

Programmable Timer/Counter Core

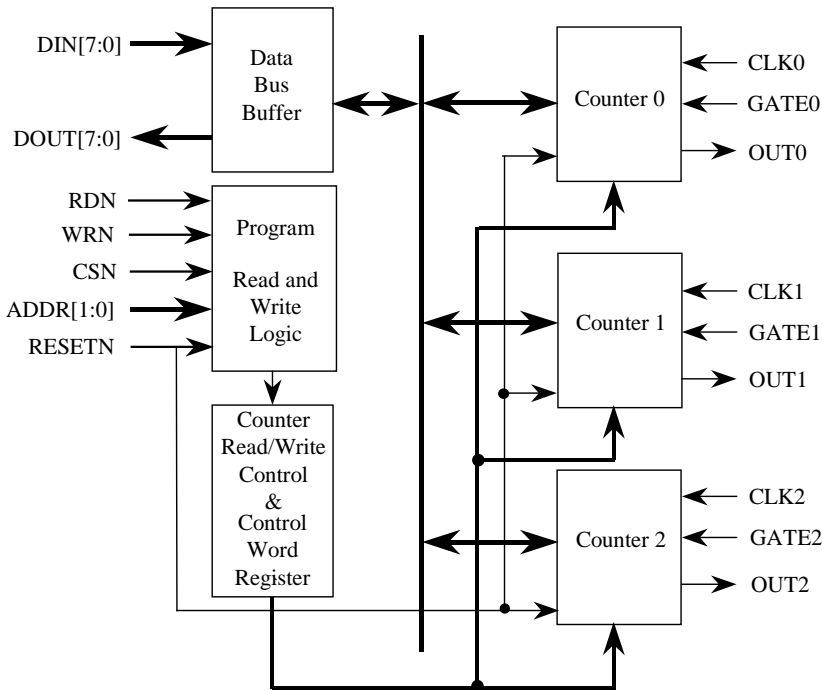
The C8254 core implements a high performance programmable interval timer/counter device, which is designed to solve the common timing control problems in microcomputer system design. It provides three independent 16-bit counters, and each counter may operate in a different mode. All modes are software programmable. The C8254 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control programmed to match the requirements by programming one of the counters for the desired delay.

Applications

The six programmable timer modes allow the C8254 to be used in applications requiring event counters including:

- elapsed time indicators
- programmable one-shots

Block Diagram



Features

- Three Independent 16-bit Counters
- Status Read-Back Command
- Counter Latch Command
- Read/Write LSB only or MSB only or LSB first then MSB
- Six Programmable Counter Modes
 - Interrupt on Terminal Count
 - Hardware Retriggerable One-Shot
 - Rate Generator
 - Square Wave Mode
 - Software Triggered Strobe
 - Hardware Triggered Strobe (Retriggerable)
- Binary or BCD Counting
- Functionality based on the INTEL 8254

Functional Description

This section provides a short description of each element of the Block Diagram.

Data Bus Buffer

8-bit input and output data bus buffer is used to interface the C8254 to the system bus.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the C8254. ADDR[1:0] select one of the three counters or the control word register to be read from or written into. A "low" on RDN tells the C8254 that the CPU is reading one of the counters. A "low" on the WRN input tells the C8254 that the CPU is writing either a Control Word or an initial count. Both RDN and WRN are qualified by CSN. RDN and WRN are ignored unless the C8254 has been selected by holding CSN "low".

Control Word Register

The Control Word Register is selected by the Read/Write Logic when ADDR[1:0] = 11. During writing, the data is stored in the Control Word Register and it is interpreted as a Control Word used to define the operation of the Counters.

Control Word Format

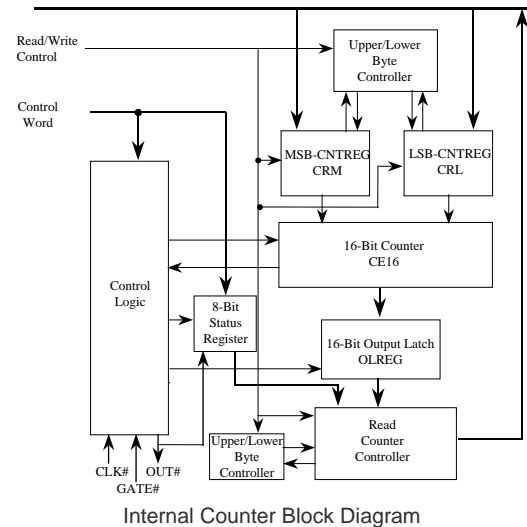
D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command

RW1	RW0	
0	0	Counter Latch Command
0	1	Read/Write LSB only
1	0	Read/Write MSB only
1	1	Read/Write LSB first, then MSB

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD	
0	Binary Counter 16-bits
1	BCD Counter (4 Decades)



Counter 0, Counter 1, Counter 2

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in the Figure above. The Counters are fully independent. Each Counter may operate in a different Mode.

Control Logic

This block controls the 16-bit counter for all counting modes and the Null flag of the counter.

Upper/Lower Byte Controller

The width of the data bus is 8 bits, and the counter is 16 bits. The Upper/Lower Byte Controller allows one 8-bit Counter Register, MSB or LSB, to be loaded one at a time from the internal bus. If the Counter is programmed for two-byte read/write mode, this block will control which data byte will be read at the next read cycle.

Counter Registers

There are two 8-bit registers called CRM and CRL. Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE16. At the rising-edge of WRN, it will write data to the register. One register at a time will be allowed to be loaded from the internal bus. After both registers have been loaded, both bytes are transferred to the CE16 simultaneously. CRM and CRL are cleared when the Counter is programmed.

Note that the CE16 can't be written into; whenever a count is written, it is written into the CR.

16-Bit Counter

This block contains a 16-bit Binary or BCD presetable synchronous down counter.

8-Bit Status Register

The 8-bit Status Register contains the Control Word Register, the status of the output and null count flag. When there is a Read-Back Command with STATUSN bit enabled and its counter selected, it will latch present status information into Status Register. The status format is shown below:

D7	D6	D5	D4	D3	D2	D1	D0
Out	Null Count	RW1	RW0	M2	M1	M0	BCD

Bits D5 through D0 contain the counter's programmed Mode. Output bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software. Null Count bit D6 indicates when the last count written to the counter register has been loaded into the counting element (CE16). The exact time this happens depends on the Mode of the counter.

8-Bit Output Latch Register

At the time of receiving the Counter Latch Command or Read-Back Command with COUNTN bit enabled, the selected counter's output latch latches the count. This count is held in the latch until the CPU reads it or until the counter is reprogrammed. The count is then unlatched and the OL returns to be transparent of counting element outputs. The count must be read according to the programmed format. The Counter Latch Command is ignored before the count is read.

Read Counter

If both the count and the status of a counter are latched, the first read operation of that counter will return the latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two byte counts) returns the latched count. Subsequent reads return the unlatched count. If the counter is programmed for two byte counts, it will read the LSB first then the MSB at the next read cycle.

Implementation Results

C8254 reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results.

Supported Family	Slices ²	BRAM	IOBs ¹	Fmax	ISE
Spartan-3E 3S1200E-5	332	-	31	75 MHz	12.2i
Spartan-6 6SLX25-5	153	-	31	110 MHz	12.2i
Virtex-5 5VLX30-3	147	-	31	198 MHz	12.2i
Virtex-6 6VLX130T-3	146	-	31	206 MHz	12.2i

Notes:

1. Assuming all core I/Os are routed off-chip
2. Optimized for area

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The C8254 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 82C54 chip, and the results compared with the core's simulation output.

Deliverables

The core includes everything required for successful implementation:

Netlist License

- Post-synthesis EDIF netlist
- Testbench (self checking)
- Vectors & expected results for testing functionality
- Place & Route scripts
- Constraints file
- Documentation

HDL Source License

- VHDL or Verilog RTL source code
- Testbenches (self checking)
- Wrapper for pin compatible replacement
- Vectors & expected results for testing functionality
- Synthesis and simulation scripts
- Documentation