

# CAST

## ATAIF

### ATA-8/IDE Host Controller Core

Implements a host controller for non-volatile memory devices using the parallel interface known as ATA (Advanced Technology Attachment), IDE (Integrated Drive Electronics), and ATAPI (Advanced Technology Attachment Packet Interface). Complies with standard ATA-8.

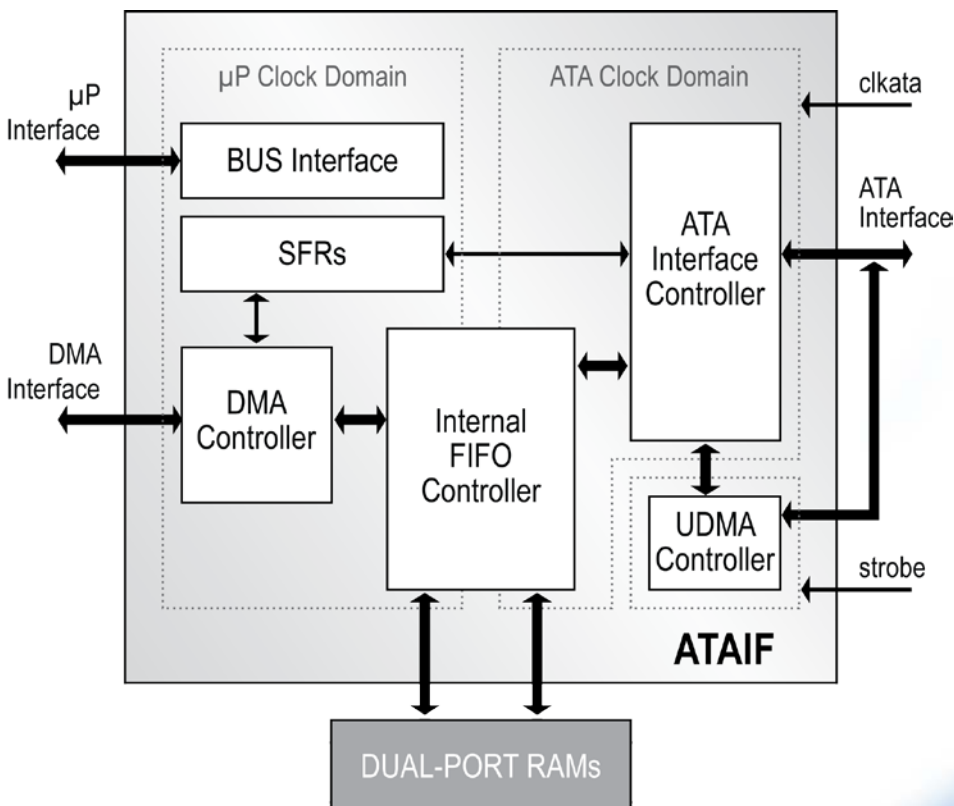
The core provides a simple interface to memory devices such as hard-disk drives, DVD players, CDROM players/writers, Compact Flash storage, and PC Card devices. It supports PIO modes 0 to 4; Multi-word DMA modes 0, 1 and 2; Ultra ATA -33, -66, -100 and -133; and implements an interface to the IDE bus.

Developed for easy reuse in ASIC and FPGA implementations, the core is strictly synchronous, with positive-edge clocking, no internal tri-states, and a synchronous reset; scan insertion is straightforward.

#### Applications

- IDE disk drive, CDROM player/writer & DVD player controllers
- Compact Flash and PC-Card readers
- Systems utilizing IDE/ATA and ATAPI drives for data storage including notebook and desktop computers, servers, set-top boxes and test equipment
- Data acquisition systems

#### Block Diagram



#### Features

- Complies with ATA-8 Standard
- Supports one or two IDE devices
- Supports synchronous Ultra ATA-33, -66, -100 and -133
- Configurable parameters allow easy tailoring of core to specific application or implementation technology
- Programmable I/O modes: 0, 1, 2 and 4
- Multi-word DMA modes: 0, 1 and 2
- Generic SFR interface with configurable data bus: 8/16/32-bit
- Configurable Internal FIFO address bus width: min. 4-bit, no upper limit
- Configurable transmission counter size: from 2- to 32-bit
- OCP, AXI, AHB, PLB and Avalon interfaces
- DMA Controller provides synchronous data transmission interface
  - Master and slave mode
  - Scatter-gather support
  - Configurable data bus: 8/16/32-bit
  - Configurable address bus: min. 8-bit, no upper limit
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)

## Functional Description

The core is partitioned into modules as shown in the block diagram and described below.

### ATA Interface Controller

Contains the PIO, MDMA and UDMA state machines. These control the ATA Interface working in PIO modes 0 to 4; Multi-word DMA modes 0, 1 and 2; and Ultra ATA -33, -66, -100 and -133 modes.

Also parallel data CRC generation for UDMA transfers.

### UDMA Controller

Contains buffers for input data, used while the core executes Ultra DMA transfers.

### DMA Controller

Used for data transmissions, working as a master or a slave system data bus (according to settings in the SFRs). The DMA controller supports scatter-gather for transfer flexibility, and burst data transfers.

### Internal FIFO Controller

Has two buffers used for buffering transmit and receive data inside the core. Generates read/write signals for two on-chip Dual-Port RAMs.

### SFRs

Contains a set of Special Function Registers used for controlling the core.

### BUS Interface

Controls the microprocessor bus interface. It provides a synchronous read/write interface to the SFRs that can be easily integrated with various processor systems.

## Implementation Results

The core has been evaluated in a variety of technologies. The following are sample ASIC pre-layout results, implemented without DRAM for the internal FIFO and using an ATA clock of 133 MHz.

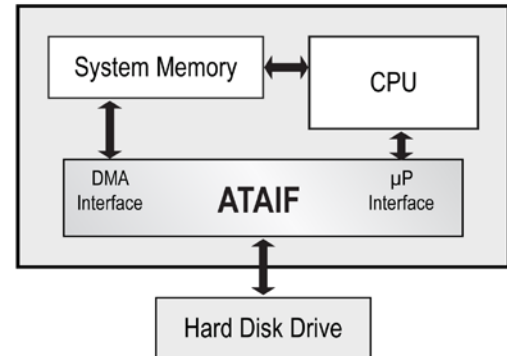
ASIC Technology	Logic Eq. Gates	Processor Bus Clock Frequency
UMC 0.18 $\mu$ m <sup>1</sup>	14,100	100 MHz
UMC 0.18 $\mu$ m <sup>2</sup>	17,400	263 MHz
UMC 0.13 $\mu$ m <sup>2</sup>	18,500	500 MHz
UMC 0.09 $\mu$ m <sup>1</sup>	18,300	50 MHz

Notes: 1 optimized for area  
2 optimized for speed, using DMA Controller, max. size data buses, and internal FIFO depth of 512 words

See the web site for FPGA implementation results.

## Example Application

Here the core is used to send data from system memory to a hard disk drive. It uses the DMA Interface, and the CPU processes interrupts and controls the settings.



## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

## Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001) including an example system design and bus/behavioral model of interface stimulators
- Simulation script, vectors and expected results
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide

## Related Products

**ATAIF-SD** - a complete software set for handling the Parallel ATA host controller. It supplements the ATAIF controller with software elements and enables smooth integration of the controller in the target application, allowing user to easily access storage media of high capacity without detailed knowledge of the controller interface.