BA22-CE

32-bit Cache-Enabled Embedded Processor

Implements a 32-bit processor for deeply embedded applications that use off-chip instruction and data memories and that may need to run a real-time operating system (RTOS). Part of the royalty-free BA22 family, this processor megafunction is extremely competitive in terms of high performance and low power consumption, and has best-in-class code density.

The megafunction has Instruction and Data Caches, optional dedicated buses for tightly coupled on-chip Instruction and Data memories, and an AMBA® AHB™ or Wishbone system bus interface. It includes up to 32 general purpose registers (GPRs), a tick-timer (TTimer), a programmable interrupt controller (PIC), an advanced power management unit (PMU), and an optional debug unit (DBGU). Additional microcontroller peripherals may be ordered for pre-integration and delivery with the megafunction, individually or in a complete platform. IP Integration Services are also available to help integrate the processor with memory controllers, image compression, or other CAST IP megafunctions.

The processor’s BA2 instruction set is relatively simple and extremely compact. Programming is facilitated with the included C/C++ tool chain, Eclipse IDE, architectural simulator, and ported C libraries.

The BA22-CE synthesizes to 25k gates, can be clocked with 400MHz in a 65nm technology, and can provide as many as 2.53 DMIPS/MHz. The megafunction is delivered, with a complete software development environment under Eclipse IDE, and its users get access to already ported real time operating systems (eCOS and uClinux).

The BA22 family of processors has been designed for easy reuse and integration, has been rigorously verified, and is production proven. Contact CAST Sales for details.

**Applications**

- Mixed signal embedded processing
- Internet, networking and telecom
- Home entertainment consumer electronics
- Portable and wireless
- Automotive

**Block Diagram**

**Features**

- High Performance 32-bit CPU
  - 2.53 DMIPS/MHz
  - 2.93 MegafunctionMarks/MHz
  - Variable length (16/24/32/48 bits) instruction encoding
  - Single-cycle instruction execution on most instructions
  - Fast and precise internal interrupt response
  - Custom user instructions

- Small Silicon Footprint & Low Power
  - Industry-leading code density
  - 15k gates and as little as 0.05W/MHz on 90nm

- Fast & Flexible Memory Access
  - Harvard-style, separate Instructions and Data caches
  - Tightly coupled Quick Memory for fast and deterministic access to code and/or data

- Efficient Power Management
  - Further reduces power consumption by 2x to 100x using dynamic clock gating for individual units
  - Software controlled clock frequency in slow and idle modes
  - Interrupt wake-up in doze and sleep modes

- Advanced Debug Capability
  - Non-intrusive debug/trace for both CPU and system
  - Complex chained watchpoint and breakpoint conditions
  - Uses industry standard Amontec JTAGKey USB to JTAG interface

- Integrated Peripherals
  - 32 bits-wide tick timer and Programmable interrupt controller

- Optional Peripherals
  - AMBA bus infrastructure
  - Microcontroller peripherals such as GPIO, UART, Real-Time Clock, and Timers
  - Serial communication megafunctions such as I2C and SPI
  - Memory controllers and more

- Easy Software Development
  - Eclipse IDE for Windows & Linux
  - C /C++ compiler, debugger, linker, assembler, and utilities
  - Architectural simulator
  - Ported libraries and RTOS
Processor Description

The BA22 family uses a 32-bit processor architecture designed for high performance with great silicon and power efficiency.

The highly configurable design may include caches and memory management units, enhanced arithmetic processing capabilities such as a divider and floating point unit, a sophisticated power management unit, and an interactive, JTAG-based debug capability.

The BA22-CE is one pre-configured version of the BA22, targeted for a variety of deeply embedded applications.

BA22 processors are also designed for quick, efficient software development. The BA2 instruction set they use provides the highest code density in its class, without compromises on performance, ease of use, or scalability. It features:

- A linear, 32-bit or 64-bit logical address space
- An instruction length of 16, 24, 36, 48, or 64 bits, which reduces memory requirements by as much as 40%.
- Simple memory addressing modes
- Configurable general purpose registers (12 to 32 GPRs)
- Efficient memory transfer instructions

The BA22 has already proven itself in multiple production designs.

Implementation Results

The following results reported from Altera tools, assume 32 GPRs, a 4x64 RAM connected to the IQEM bus, an 8x32 RAM connected to the DQEM bus, a 8Kbytes 2-way associative instruction cache, a 2Kbytes 2-way associative data cache, that all clocks are driven by a common source, and that all megafunction I/Os are routed off-chip.

<table>
<thead>
<tr>
<th>Family</th>
<th>Device</th>
<th>Logic Area</th>
<th>Memory*</th>
<th>Clock (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cyclone IV-E EP4CE75F29C7</td>
<td>8,778 LEs</td>
<td>84 M9K</td>
<td>58</td>
<td></td>
</tr>
<tr>
<td>Cyclone V** 5CGXFC7D6F31C8</td>
<td>4,696 ALUTs</td>
<td>84 M10K</td>
<td>90</td>
<td></td>
</tr>
<tr>
<td>Stratix IV EP4SE820H35C3</td>
<td>5,437 ALUTs</td>
<td>82 M9K</td>
<td>131</td>
<td></td>
</tr>
<tr>
<td>Stratix V 5SGXMA7H1F35C1</td>
<td>5,203 ALUTs</td>
<td>50 M20K</td>
<td>153</td>
<td></td>
</tr>
</tbody>
</table>

* Memory required for the implementation of QMEMs and Caches, not the CPU.
** Cyclone-V implementation does not include the debug unit.

The provided figures do not represent the higher speed or smaller area for the megafunction. Area, power and speed depend on megafunction configuration and tool optimizations. Furthermore power consumption depends on power management, software and memories configuration. For accurate characterization on your application please contact CAST.

Support and Services

The megafunction as delivered is warranted against defects for 90 days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

IP Integration Services are also available to help minimize time to market for BA22-Based systems.

Deliverables

The megafunction is available in synthesizable HDL or targeted netlist, and includes everything required for successful implementation:

- Verilog RTL source code or targeted netlist
- Verilog Testbench
- Silicon-proven Reference SoC/ASIC Design
- Software development tools for Cygwin on Windows and Linux, with Eclipse IDE interface
- Operating systems and board support package

A reference design board running Linux and FPGA versions of the megafunction are also available; contact CAST Sales for information.

Related Products

The BA2x™ Processor Family includes a set of royalty-free, pre-configured products intended for different applications:

- **BA25** 32-bit Application Processor, for demanding systems running applications on general-purpose operating systems such as Linux and Android.
- **BA22-AP** 32-bit Basic Application Processor, for embedded applications that may need to run a full OS.
- **BA22-DE** 32-bit Deeply Embedded Processor, for deeply embedded applications that use on-chip instruction and data memories.
- **BA21** 32-bit Low-Power Deeply Embedded Processor, implements a 32-bit low-power processor that delivers better performance than most processors of its size.

Platforms

- **BA2x-AXi-PP** Pre-integrated peripherals platform for the AMBA3 AXI bus.
- **BA2x-AHB-PP** Pre-integrated peripherals platform for the AMBA2 AHB/APB buses.