

# CAST



## C80186XL

### 80186XL-Compliant Chip Replacement 16-bit Microcontroller Core

A semiconductor IP core that implements a pin-compatible replacement for the Intel® 80C186XL chip.

This 80186XL ISA compliant 16-bit microcontroller is a single-chip, high-performance design that executes the widely-known instruction set of Intel 80c86 or 80c186 devices. It has the extended peripherals set of the 80C186XL: three timers, a refresh control units, and two direct memory access (DMA) channels.

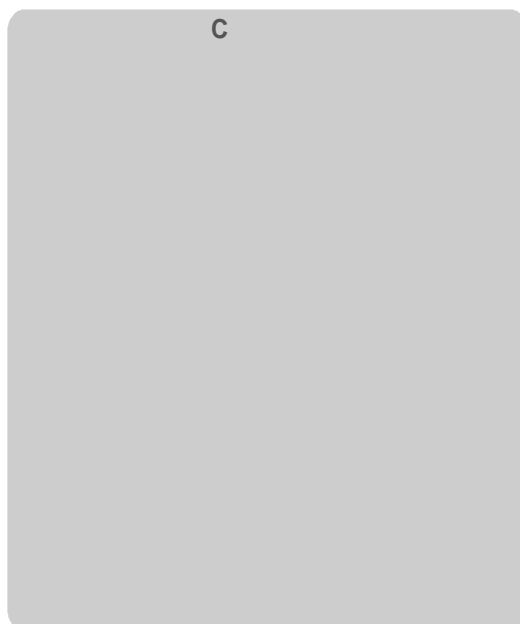
Compatibility with the original chip was ensured using hardware modeler-based reverse engineering. Software written for the original chip should execute on the C80186XL with little or no additional effort. A set of flexible outputs makes it easy to ensure pin-to-pin compatibility using current ASIC, Structured ASIC, or FPGA fabrication technologies, making obsolete part replacement straightforward and cost-effective for either low- or high-volume applications.

The microcode-free core design is strictly synchronous, with positive-edge clocking, no internal tri-states, and a synchronous reset; therefore scan insertion is straightforward.

### Applications

The C80186XL is designed for obsolete parts replacement, but can also serve well in embedded systems or as a new controller (because it requires little extra support from a chipset). Suitable 16-bit applications include high-speed control systems, microcomputer systems, automotive controls, and audio and video controls.

### Block Diagram



### Features

- Control Unit:
  - 9-level deep and 1-byte wide instruction queue
  - Independent instruction execution stages allow instructions to overlap
- Arithmetic Logic Unit:
  - 16-bit arithmetic and logical operations
  - Boolean manipulations
  - 16 x 16-bit multiplication and 32-/16-bit division
- Memory Interface:
  - compliant with the 80c186xl device
  - 20-bit addressing space
  - 1MB memory space divided into 64KB logical segments
  - Internal and external control of the length of memory access to instruction and data
  - 64KB IO space
- Chip Select Unit with ten chip select outputs for use with memory devices
- Peripheral Control Block:
  - 128 16-bit wide words predefined for peripherals control
  - Programmable into memory or IO space
- Power Management Unit enabling clock division by a factor of 1, 4, 8, or 16
- Three 16-bit Timers/Counters
- Direct Memory Access (DMA) Controller:
  - Two separate, fully-functional DMA channels
  - External transfer initiation by DRQn pins
  - Linear access to 20-bit memory addressing space
- Programmable Interrupt Controller:
  - Five external interrupt lines, including NMI
  - Five internal interrupts generated by the peripherals set
- Refresh Control Unit
- Strictly synchronous design with no internal tri-states

## Functional Description

The C80186XL core is partitioned into modules as shown in the figure above and described below.

### C80186XL CPU

This module consists of several smaller parts. Arithmetic Logic Unit (ALU) is capable of conducting 16-bit arithmetic and logic operations as well as arithmetic and logic shift operations. Multiplication Division Unit (MDU) increases performance and flexibility of the core by executing 16X16 multiplication, and 32/16 division (signed and unsigned). The control subcomponent contains the instruction decoder and the main Finite State Machine (FSM), while Queue part, eight bits wide and five levels deep, fetches all instructions and immediate data. The C80186CPU has the control logic for memory interface, as well as various registers: general purpose (AX, BX, CX, DX), segment (CS, SS, DS, ES), index (SI, DI), base pointer (BP, SP) and status (PSW) one.

### ITU — Integrated Timer Unit

Has three programmable 16-bit Timers/Counters. Timers 0 and 1 are versatile timers and external event counters, each with two external pins, input and output. Timer 2 is for internal use only, such as generating delays.

### PCB — Peripheral Control Block

Manages communication between the CPU and internal peripherals.

### CSU — Chip Select Unit

A set of comparators used to activate the appropriate chip select signal, depending on a current address and the control registers configuration. It also generates an internal acknowledge signal, depending on an external acknowledge signal and internally-generated wait states.

### RCU — Refresh Control Unit

Generates refresh addresses for external DRAM memory, with refresh request time intervals programmable by a 9-bit register.

### DMA0 & DMA1 — Direct Memory Access Channels

Two independent DMA channels with a 20-bit linear address space (no segmentation) and maximum transfer count up to 65536 transfers. Transfer size can be either a byte or a word. Both DMAs have access to memory and/or I/O space as well as two priority levels. Requests from three sources can be handled: Timer2, the external DRQn pin, and software transfer initialization. There are also three channel synchronization modes— independent incrementation/decrementation/none addressing modes for each channel and each direction—plus interrupt generation for each channel. The fastest possible memory transfer takes two bus accesses (read and write).

## ICU — Interrupt Controller

Serves up to five external sources (including NMI) with programmable edge or level triggering for external sources (INT0 – INT3 only). Five interrupts are connected from internal sources—two from the DMA channels and three from timer units—each with both programmable priority and individual masking. Nesting of interrupt sources is also handled within this module. Also handles polled operations, and cascading with external i8259a modules to expand the number of external interrupt sources.

## PWRMAN

Gathers logic related to clock generation, clock divide, and reset generation. Since this type of logic can be technology-dependent, PWRMAN is outside the core.

## Example Application



The 80186XL architecture suits low-power applications, such as this portable photo viewer. Images can be acquired from the USB and Firewire devices, and displayed on an LCD screen using the VGA Controller. NAND Flash memory stores the application firmware and its upgrades, while DRAM facilitates data exchange between system components. A C80187 numeric coprocessor improves system performance by accelerating floating-point calculations inside the CPU.

## Implementation Results

C80186XL reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results using optimization for area.

Xilinx Technology	Area (Slices)	BRAM	IOB	Frequency	ISE Version
Virtex-4 XC4VLX15-12	5324	-	63	177 MHz	10.1.02
Virtex-5 XC5VLX30-3	2490	-	63	150 MHz	10.1.02
Spartan-3E XC3S1200E-5	5147	-	63	110 MHz	10.1.02
Spartan-6 XC6SXL25-2	2527	-	63	45 MHz <sup>1</sup>	12.2

<sup>1</sup> Optimized for area

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The C80186XL core's instruction set functionality as well as the peripherals set were verified by means of a proprietary Personal Hardware Modeler. The same instructions and test scenarios were put as stimulus to a hardware model that contained the original Intel 80c186xl chip and the results of the operations were compared with the core's simulation output. Subsequently, pin-to-pin compatibility was achieved.

## Deliverables

The core includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Example CHIP80186XL module.  
This chip level design uses the C80186XL IP core and illustrates how to build the module that is the pin replacement of the 80c186xl device
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide