

CAST



C80186EC

80186EC-Compliant Chip Replacement 16-bit Microcontroller Core

A semiconductor IP core that implements a pin-compatible replacement for the Intel® 80C186EC chip.

This 80186EC ISA compliant 16-bit microcontroller is a single-chip, high-performance design that executes the widely-known instruction set of Intel 80c86 or 80c186 devices. It has an extended peripheral set: three timers, two serial units, a watchdog timer, two universal interrupt controllers (8259a) and four DMA channels.

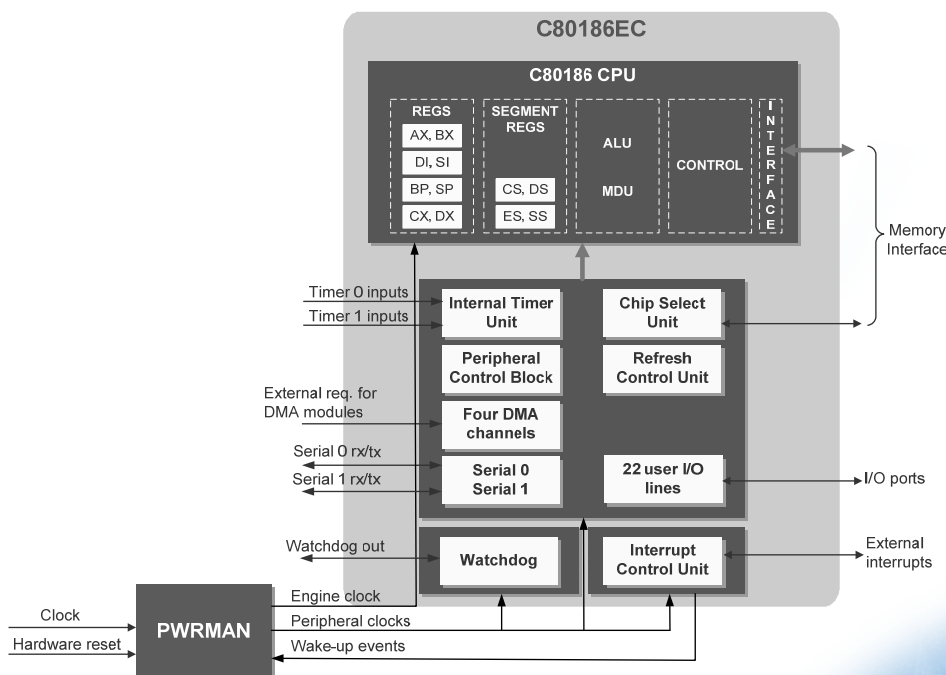
Compatibility with the original chip was ensured using hardware modeler-based reverse engineering. Software written for the original chip should execute on the C80186EC with little or no additional effort. A set of flexible outputs makes it easy to ensure pin-to-pin compatibility using current ASIC, Structured ASIC, or FPGA fabrication technologies, making obsolete part replacement straightforward and cost-effective for either low- or high-volume applications.

The microcode-free core design is strictly synchronous, with positive-edge clocking, no internal tri-states, and a synchronous reset; therefore scan insertion is straightforward.

Applications

The C80186EC is designed for obsolete parts replacement, but can also serve well in embedded systems or as a new controller (because it requires little extra support from a chipset). Suitable 16-bit applications include high-speed control systems, microcomputer systems, automotive controls, and audio and video controls.

Block Diagram



Features

- Control Unit:
 - 9-level deep and 1-byte wide instruction queue
 - Independent instruction execution stages allow instructions to overlap
- Arithmetic Logic Unit:
 - 16-bit arithmetic and logical operations
 - Boolean manipulations
 - 16 x 16-bit multiplication and 32-/16-bit division
- Memory Interface:
 - compliant with the 80c186ec device
 - 20-bit addressing space
 - 1MB memory space divided into 64KB logical segments
 - Internal and external control of the length of memory access to instruction and data
 - 64KB I/O space
- Chip Select Unit with ten chip select outputs for use with memory devices
- Peripheral Control Block:
 - 128 16-bit wide words predefined for peripherals control
 - Programmable into memory or I/O space
- Power Management Unit enabling clock division by a factor of 1, 4, 8, 16, 32 and 64 factors
- Three 16-bit Timers/Counters
- Watchdog Timer
- Direct Memory Access (DMA) Controller:
 - Four separate, fully-functional DMA channels
 - External transfer initiation by DRQn pins
 - Linear access to 20-bit memory addressing space
- Two USART Peripheral Interfaces in full duplex mode
 - Synchronous and asynchronous transmission
 - Full-duplex operation
 - 7-, 8- or 9-bit data transfers
 - Odd, even, or no parity
 - Clear to send feature in transmission
 - Double buffered TX/RX

Features (Continued)

- Programmable Interrupt Controller:
 - Two internally cascaded 8259a interrupt controllers
 - Nine external interrupt lines, including NMI
 - Seven internal interrupts generated by peripherals
- Refresh Control Unit
- Strictly synchronous design with no internal tri-states

Functional Description

The C80186EC core is partitioned into modules as shown in the figure above and described below.

C80186 CPU

This module consists of several smaller parts. Arithmetic Logic Unit (ALU) is capable of conducting 16-bit arithmetic and logic operations as well as arithmetic and logic shift operations. Multiplication Division Unit (MDU) increases performance and flexibility of the core by executing 16X16 multiplication, and 32/16 division (signed and unsigned). The control subcomponent contains the instruction decoder and the main Finite State Machine (FSM), while Queue part, eight bits wide and five levels deep, fetches all instructions and immediate data. The C80186CPU has the control logic for memory interface, as well as various registers: general purpose (AX, BX, CX, DX), segment (CS, SS, DS, ES), index (SI, DI), base pointer (BP, SP) and status (PSW) one.

Internal Timer Unit

Has three programmable 16-bit Timers\Counters. Timers 0 and 1 are versatile timers and external event counters, each with two external pins, input and output. Timer 2 is for internal use only, such as generating delays.

Chip Select Unit

A set of comparators used to activate the appropriate chip select signal, depending on a current address and the control registers configuration. It also generates an internal acknowledge signal, depending on an external acknowledge signal and internally-generated wait states.

Peripheral Control Block

Manages communication between the CPU and internal peripherals.

Refresh Control Unit

Generates refresh addresses for external DRAM memory, with refresh request time intervals programmable by a 9-bit register.

Four DMA Channels

The Direct Memory Access unit is comprised of two identical modules with two DMA channels each. The DMA transfers allow for data copying without processor intervention. The DMA unit can be configured for transfer from/to different addresses and from/to memory or the I/O space, with the address increment/decrement option different for the source and the destination.

Serial 0 / Serial 1

The Serial Unit is comprised of two identical serial ports; each serial port operates independently from the other. The serial interfaces provide flexible, full-duplex synchronous/asynchronous receiver/transmitter operations. Each module can operate in five modes: one synchronous and four asynchronous. Both serial units are buffered at the receive side, and also at the transmit side.

Watchdog

The Watchdog Timer Unit can preserve a system from an unexpected software dead loops or/and critical system errors. This module contains a down counter that should be reloaded periodically or it signals underflow, such event can be used to interrupt the microcontroller or cause a system reset

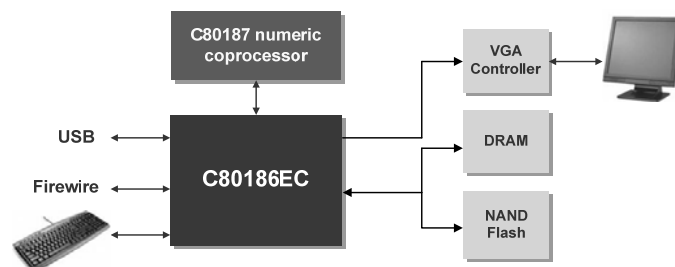
Interrupt Controller

The Interrupt Controller is composed of two 8259A modules connected in cascade fashion. Each instance of the 8259A module is implemented as an independent IP compatible with the Intel® 8259A chip.

PWRMAN

Gathers logic related to clock generation, clock divide, and reset generation. Since this type of logic can be technology-dependent, PWRMAN is outside the core.

Example Application



The 80186EC architecture suits low-power applications, such as this portable photo viewer. Images can be acquired from the USB and Firewire devices, and displayed on an LCD screen using the VGA Controller. NAND Flash memory stores the application firmware and its upgrades, while DRAM facilitates data exchange between system components. A C80187 numeric coprocessor improves system performance by accelerating floating-point calculations inside the CPU.

Implementation Results

C80186EC reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results including memory.

Xilinx Device	Slices	BRAM	Special Features	I/Os	Fmax (MHz)	ISE
Spartan-3E 3S1600E-5	7,827	-	1 MULT	85	33	10.1i
Virtex-4 4VLX25-12	7,249	-	1 DSP	85	52	10.1i
Virtex-5 5VLX30-3	3,535	-	1 DSP	85	60	10.1i

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The C80186EC core's instruction set functionality as well as the peripherals set were verified by means of a proprietary Personal Hardware Modeler. The same instructions and test scenarios were put as stimulus to a hardware model that contained the original Intel 80c186ec chip and the results of the operations were compared with the core's simulation output. Subsequently, pin-to-pin compatibility was achieved.

Deliverables

The core includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Example CHIP80186EC module.
This chip level design uses the C80186EC IP core and illustrates how to build the module that is the pin replacement of the 80c(l)186ec device
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide