

# CAST

## C68000

### 16-bit Microprocessor Core

The C68000 is core of a powerful 16/32-bit microprocessor and is derived from the Motorola MC68000 microprocessor. The C68000 is a fully functional 32-bit internal and 16-bit external equivalent for the MC68000. The C68000 serves interrupts and exceptions, and provides an interface for M6800 family peripherals.

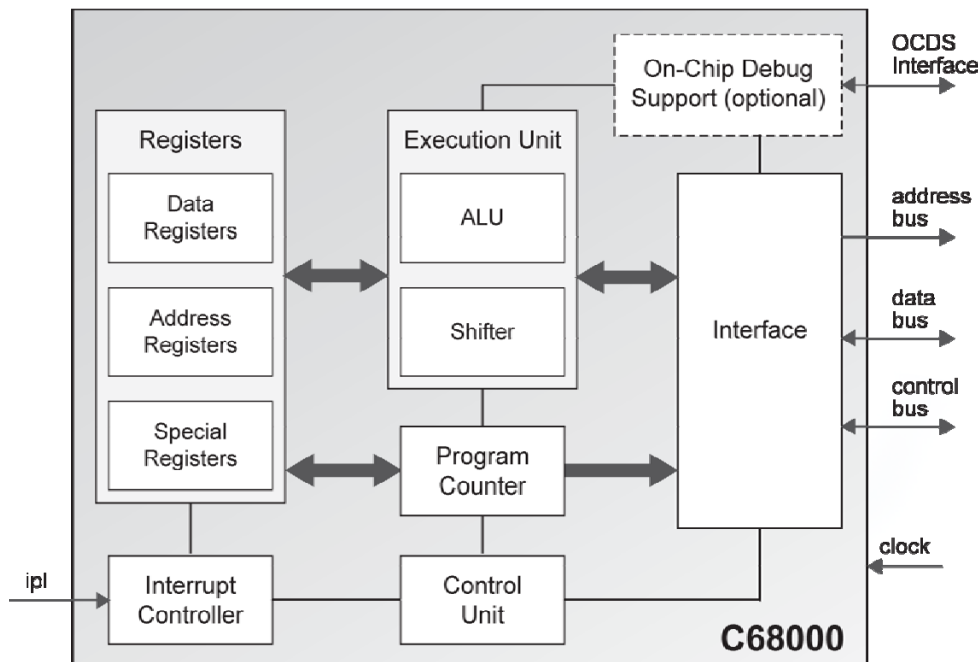
The C68000 is the microcode-free design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous without internal tri-states and with a synchronous reset. Scan insertion is straightforward.

### Applications

The C68000 can be utilized for a variety of applications including:

- Microcomputer systems
- Embedded microcontroller systems
- Data computation and transfer
- Communication systems
- Professional audio and video

### Block Diagram



### Features

- Control Unit
  - 16-bit two levels instruction decoder
  - Three levels instruction queue
- 55 instructions and 14 address modes
- Supervisor and User mode
  - Independent stack for both modes
- Users registers
  - Eight 32-bit data & address registers
  - 16-bit status register
- Data format
  - Integer 8, 16 or 32-bit
  - BCD packet
  - Bit
- Memory interface
  - Independent data and address buses
  - Asynchronous bus control
  - 4 GB-address space
  - 31-bit address bus (optional 32-bit)
  - 8-address spaces (used 5)
  - 16-bit data bus
- Interrupt Controller
  - Seven Priority Levels
  - Unlimited interrupt sources
  - Vectored or auto-vectored interrupt modes
- Arithmetic-Logic Unit
  - 8, 16, 32-bit arithmetic and logic operations
  - Boolean manipulations
  - 16 x 16-bit multiplication (sign or unsigned)
  - 32 / 16-bit division (sign or unsigned)
- M6800 peripherals family synchronous interface
- Two or Three wire bus arbitration interface
- Operation execution is the same for data or address registers
  - No different for operation on data or address registers
- EASE debugging environment
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)

## Functional Description

The C68000 core is partitioned into modules as shown above and described below.

### Execution Unit

Arithmetic-Logic Unit. (ALU) performs:

- 32-bit arithmetic operations
- 32-bit logic operations
- Bit manipulations

Address/Data Shifter performs various types of shift and rotate operations by one bit position.

These two units with some additional logic, allows all basic operation on data and address registers.

### Program counter

The program counter (PC) is 32 bits wide. This register can be incremented or loaded by the control unit during instruction execution.

### Main control

Decodes and executes instructions. Contains main processor sequencer and control unit for all inner resources.

### Registers

The C68000 has eight 32-bit data registers, eight 32-bit address registers, one 32-bit user stack pointer and a 16-bit status register. Data registers are mainly used for data operations but can also be used as index registers. Address registers can be used as software stack pointers, index registers or base address registers. Status register contains operations results flags, and system control bits.

### Interrupt control

Provides seven priority levels of interrupt and calculates an internal vector during the auto-vector interrupt. It also holds the internal state of the interrupt and exception level.

### Interface

Manages all accesses to memory. Generates all control signals to memory and peripherals. This is a synchronous device working with both rising and falling edge of the *clk* (clock) signal.

### OCDS

Serves as the interface for On-Chip Debug Support using an IEEE1149.1 (JTAG) port. The OCDS unit provides the following functions - run/stop control, single-step mode, software/hardware breakpoints, debugger program execution and Read/Write Access to all memory space.

## Implementation Results

C68000 reference designs have been evaluated in a variety of technologies. The following are sample ASIC results.

Device	Optimized for	Area	Speed
UMC 0.18	speed	26,250 gates	238 MHz
UMC 0.13	area	22,674 gates	66 MHz

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. All subcomponents were functionally verified with an HDL testbench using their individual test suites. The CPU and ALU have been verified against a proprietary hardware modeler and behavioral models. The peripherals have also been verified in their own testbenches, based on either hardware or behavioral models.

## Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code (ASICs) or post-synthesis EDIF netlist (FPGAs)
- Vectors for testing the core
- Sophisticated self-checking HDL Testbench (Verilog versions use Verilog 2001) including external FIFOs, buffers, models of interfaces, and the core
- Simulation script, vectors, expected results, and comparison utility
- Constraint file
- Instantiation templates
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide