

# CAST



## C68000-AHB

### 32-bit Microprocessor Core

Implements a powerful 32-bit microprocessor is derived from the Motorola MC68000 microprocessor. The core uses an AMBA-compatible AHB master interface, making it an ideal processor solution for low-cost, AHB-based System on Chip (SoC) applications.

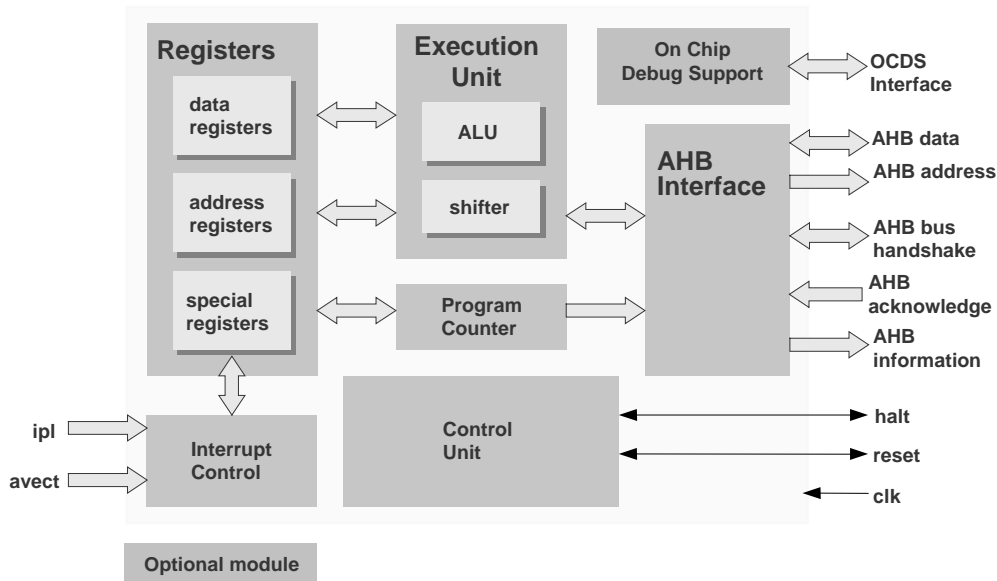
The C68000-AHB is a microcode-free design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous without internal tri-states and with a synchronous reset. Scan insertion is straightforward. Native On-Chip Debugging Support (OCDS) is available as an option to facilitate embedded processor debugging.

### Applications

The C68000-AHB is suitable for a variety of applications, including:

- 32-bit data processing applications
- High speed control systems
- Embedded microcontroller systems
- Professional audio and video
- Sensor applications

### Block Diagram



### Features

- Control Unit
  - 16-bit two levels instruction decoder
  - Three levels instruction queue
- 55 instructions and 14 address modes
- Supervisor and User mode
  - Independent stack pointer for each mode
- Users registers
  - Eight 32-bit data & address registers
  - 16-bit status register
- Data format
  - Integer 8, 16 or 32-bit
  - BCD packet
  - Bit
- Memory interface – AHB Master
  - Independent data and address buses
  - 4 GB-address space
  - 32-bit address bus
  - 32-bit data bus
  - OK, RETRY, SPLIT, ERROR responses served
  - Only NONSEQ access used
  - Bus locking for TAS instruction
  - Parameterizable endianness
- Interrupt Controller
  - Seven Priority Levels
  - Virtually an unlimited number of interrupt sources
  - Vectored or auto-vectored interrupt modes
- Arithmetic-Logic Unit
  - 8, 16, 32-bit arithmetic and logic operations
  - Boolean manipulations
  - 16 x 16-bit multiplication (sign or unsigned)
  - 32 / 16-bit division (sign or unsigned)
- Operation execution is the same for data or address registers
- Interface for On-Chip Debug solution (optional)

## Functional Description

The C68000-AHB core is partitioned into modules as shown in the block diagram and described below.

### Control Unit

Decodes opcodes and controls instruction data flow. Contains the main processor sequencer and control unit for all inner resources.

### Interrupt control

Provides seven priority levels of interrupt and calculates an internal vector during the auto-vector interrupt. It also holds the internal state of the interrupt and exception level.

### Registers

Contains eight 32-bit wide data register, eight 32-bit wide address registers, one 32-bit user stack pointer and one 16-bit status register.

### Execution unit

Contains the ALU unit for arithmetic and logic operations, and a shifter for shift operations.

### Program counter

The program counter (PC) is 32 bits wide. This register can be incremented or loaded by the control unit during instruction execution.

### AHB Interface

This interface unit implements the functionality of an AHB master. It is compliant with the AMBA bus specification rev. 2.0 and supports a 32-bit address and data busses.

All AHB responses (OK, RETRY, SPLIT, and ERROR) are served, but only NONSEQ access type is implemented.

The AHB bus clock may be faster than the CPU clock, and has a major influence on the CPU's performance. Both clocks must be synchronous, so the CPU clock has to be equal the AHB clock divided in the ratios 1:1; 1:2; 1:3; 1:4 etc.

### OCDS (optimal)

This unit provides an interface for optional On-Chip Debug support through an IEEE1149.1 (JTAG) port. The unit provides the following functions:

- Run/stop control
- Single-step mode
- Software breakpoint
- Debugger program execution
- Hardware breakpoints
- Read/Write Access every memory space

## Implementation Results

C68000-AHB reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results with the implementation constrained for clock speed including OCDS.

Xilinx Technology	Area (slices)	BRAM	Hclk	uP clock	ISE Version
Spartan-3E XC3S1200E-5	3467	-	101 MHz	50 MHz	12.2i
Spartan-6 XC6SLX25-3	1636	5	125 MHz	62 MHz	12.2i
Virtex-5 XC5VLX50-3	4323	-	250 MHz	125 MHz	12.2i
Virtex-6 XC6SLX75T-3	1456	5	251 MHz	125 MHz	12.2i

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The C68000-AHB core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Motorola MC68000 chip, and the results compared with the core's simulation outputs.

## Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Sophisticated HDL Testbench including AHB bus arbiter, AHB analyzer, configurable interrupt controller, and RAM.
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide