

CAST

C65C02

65C02-Compatible Microprocessor Core

This 65C02 IP core implements a fast, 8-bit microprocessor that executes the same instruction set as the 65C02 microprocessor. The 65C02 is an upgraded version of the popular MOS Technology 6502 8-bit CPU, and was used in many successful products such as the Apple IIc home computer.

The core provides software and hardware interrupts for interfacing external devices. With sixteen addressing modes—including indirect index and zero page—the C65C02 is able to address up to 64KB of external memory with two-byte-long instructions.

The 8-bit arithmetic logic unit can operate on signed and unsigned binary numbers as well as binary-coded decimal numbers.

The C65C02 core offer two instruction to save power by (STP) halt processor and (WAI) wait for interrupt instruction.

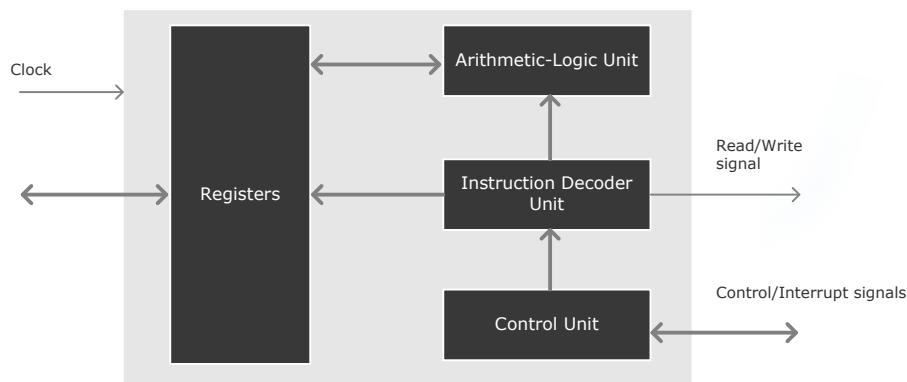
The popularity of the 6502 architecture means a significant amount of industry-certified software is ready to use with this core. The core also enables modification of the original instruction set to better suit new systems and applications.

Applications

The C65C02 core is a suitable chip replacement for extending the lifetime of existing systems, affording independence from any particular chip manufacturer. The core can also serve as an effective embedded processor for many new applications in ASIC or FPGA SoCs, including:

- 8-bit data processing applications
- Low-power consumption applications
- High-speed control systems

Block Diagram



Features

- Conforms to spec and runs instruction set of original 65C02
- Wait cycles to access slow ROM
- Single clock per cycle, whereas the average cycle number is 2

Control Unit:

- Maskable interrupt
- Non-maskable interrupt
- Set overflow flag for external numeric processing device
- Synchronization signal for single cycle execution
- Ready state input for DMA interfacing
- Vector Pull output indicates when interrupt vectors are being addressed
- Memory Lock output indicates when instruction perform Read-Modify-Write operation

8-bit Instruction Decoder:

- 69 instructions
- 212 operation codes

8-bit Arithmetic-Logic Unit:

- Decimal and binary arithmetic operations
- Logical operations
- Logical shift operations

External Memory Interface:

- Addressing up to 64 KB of:
 - External Program Memory
 - External Data Memory
 - External Input/Output space
- 16 addressing modes
- De-multiplexed Address/Data Bus to allow easy connection to memories
- RDY signal for interfacing with slow RAM/ROM modules or DMA

Power Saving Features:

- Wait for interrupt instruction
- Halt processor instruction

Functional Description

The C65C02 core is partitioned into modules as shown in figure above and described below.

Control Unit

Controls the behavior of the microprocessor by triggering interrupt subroutines and holding the microprocessor during ready signal low. It also distributes the reset signal to all other units. The control unit contains the processor status register.

Instruction Decoder Unit

Decodes every executed instruction. It provides control signals for the register unit and the arithmetic-logic unit. Besides control signals, the instruction decoder unit holds current FSM state in the state register.

Arithmetic-Logic Unit

Performs 8-bit binary and decimal addition/subtraction with carry/borrow, as well as logic operations AND, OR, XOR, shift, and rotate. Other operations include increment/decrement, bit test, and compare.

Registers Unit

All general purpose registers and special purpose registers are placed in the register unit. This includes: accumulator A, index X, index Y, program counter register, the stack pointer register and the data input and output registers. Each register in this unit is connected to the C65C02 global clock input and global synchronous reset signal.

Example Application

This figure shows typical application of the C65C02 core.

The example application uses the Commodore C64 home computer board with the C65C02 IP core. The main board is equipped with:

- VIC – Video Interface Chip
- SID – Sound Interface Device
- CIA – Complex Interface Adapter

Implementation Results

C65C02 reference designs have been evaluated in a variety of technologies. The following are sample ASIC results optimized for area.

Device	Area	Speed
TSMC 90nm	2950 gates	100 MHz

Support

The core, as delivered, is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, beginning with the first interaction. Additional maintenance and support options are available.

Verification

Functionality of the C65C02 was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original 65C02 chip, and the results compared with the core simulation outputs.

Deliverables

The core includes everything required for successful implementation:

- HDL RTL source code (soft core) or a post-synthesis EDIF netlist (firm core)
- An example C65C02 application
- Sophisticated HDL Testbench including external RAM, clock generator, and the core
- Simulation script, vectors, expected results, and comparison utility
- Synthesis (soft) or place and route (firm) script
- Comprehensive user documentation, including detailed specifications and a system integration guide

