

CAST

C6502

MOS Technology®
6502-compatible
Microprocessor Core

This 6502 IP core implements a fast, 8-bit microprocessor that executes the same instruction set as the MOS Technology 6502. It also conforms to the popular 6510 and 6502C variations of the 6502.

The core provides software and hardware interrupts for interfacing external devices. With thirteen addressing modes—including indirect-index and zero-page modes—the C6502 is able to address up to 64KB of external memory with two byte-long instructions.

The 8-bit arithmetic-logic unit can operate on signed and unsigned binary numbers as well as binary-coded decimal numbers.

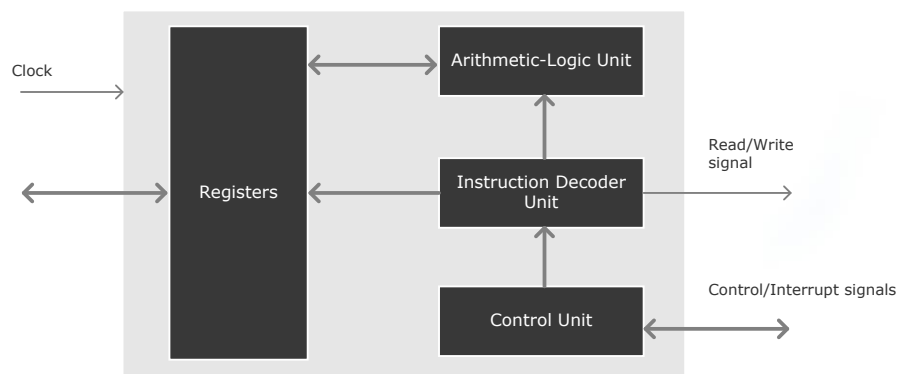
The popularity of the 6502 architecture means a significant amount of industry-certified software is ready to use with this core. The core also enables modification of the original instruction set to better suit new systems and applications.

Applications

The C6502 core is a suitable chip replacement for extending the lifetime of existing systems, affording independence from any particular chip manufacturer. The core can also serve as an effective embedded processor for many new applications in ASIC or FPGA SoCs, including:

- 8-bit data processing applications,
- Low-power consumption applications, and
- High-speed control systems.

Block Diagram



Features

- Conforms to spec and runs instruction set of original MOS Technology 6502
- Also conforms to 6510 (Commodore C64) and 6502C (Atari 130XE) variations
- Included wait cycles to access slow ROM

Control Unit:

- Maskable interrupt
- Non-maskable interrupt
- Set overflow flag for external numeric processing device
- Synchronization signal for single cycle execution
- Ready state input for DMA interfacing

8-bit Instruction Decoder:

- 56 instructions
- 151 operation codes

8-bit Arithmetic-Logic Unit:

- Decimal and binary arithmetic operations
- Logical operations
- Logical shift operations

External Memory interface:

- Addressing up to 64 KB of:
 - External Program Memory
 - External Data Memory
 - External Input/Output space
- 13 addressing modes
- De-multiplexed Address/Data Bus to allow easy connection to memories
- RDY signal for interfacing with slow RAM/ROM modules or DMA

Performance

- The C6502 uses a single clock per cycle, whereas the average cycle number is 2.

Functional Description

The C6502 core is partitioned into modules as shown in the block diagram and described below.

Control Unit

Controls the behavior of the microprocessor by triggering interrupt subroutines and holding the microprocessor during ready signal low. It also distributes the reset signal to all other units. The control unit contains the processor status register.

Instruction Decoder Unit

Decodes every executed instruction. It provides control signals for the register unit and the arithmetic-logic unit. Besides control signals, the instruction decoder unit holds the current FSM state in the state register.

Arithmetic-Logic Unit

Performs 8-bit binary and decimal addition/subtraction with carry/borrow, as well as logic operations AND, OR, XOR, shift and rotate. Other operations include increment/decrement, bit test, and compare.

Registers Unit

All general purpose registers and special purpose registers are placed in the register unit. This includes: accumulator A, index X, index Y, program counter register, the stack pointer register, and the data input and output registers. Each register in this unit is connected to the C6502 global clock input and global synchronous reset signal.

Implementation Results

C6502 reference designs have been evaluated in a variety of technologies. The following are sample ASIC results optimized for area.

Device	Area	Speed
TSMC 90nm	2066 gates	100 MHz

Support

The core, as delivered, is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, beginning with the first interaction. Additional maintenance and support options are available.

Verification

The C6502 functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original 6502 MOS Technology chip, and the results compared with the core simulation outputs.

The core has been developed according to requirements of Reuse Methodology Manual and it has achieved high score of VSIA Quality IP Assessment.

The C6502 has been verified through extensive functional simulation and it has achieved high Code Coverage simulation results.

Product Variations

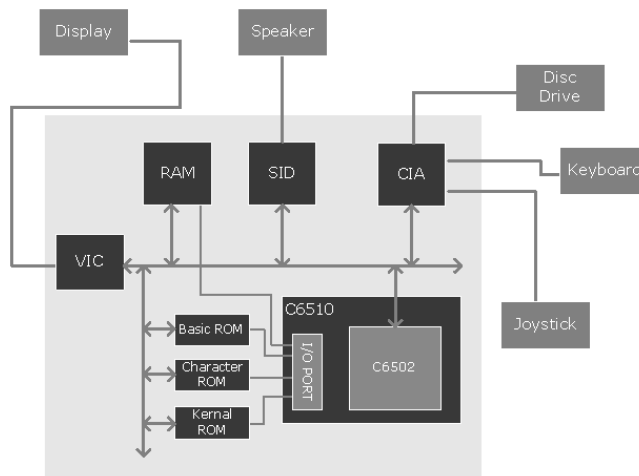
The core also supports these 6502 variations:

6510 – a 6502 microprocessor equipped with parallel bidirectional port, used in Commodore C64 home computers.

6502C – a 6502 microprocessor equipped with a HALT signal to control tri-state output buffers, used in the Atari 130XE.

Example Application

This figure shows a typical application of the C6502 core.



The core is implemented with internal I/O port and tri-state buffers as in the related C6510.

The example application uses Commodore C64 home computer board with the C6502 IP core. The main board is equipped with:

- VIC – Video Interface Chip
- SID – Sound Interface Device
- CIA – Complex Interface Adapter

Deliverables

The core includes everything required for successful implementation. The ASIC version includes:

- HDL source code
- An example C6502 application
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide