



## Functional Description

The core accepts incoming data from the 32-bit AHB bus in three common video formats: RGB 24 bits per pixel, RGB 15 bits per pixel and 4:2:2 YCbCr. It converts the video data and generates an 8-bit 4:2:2 YCbCr data stream plus all the required control signals. These include horizontal and vertical synchronization signals, and the video blanking signal.

The core interfaces its video data conversion functions with an AMBA AHB-based microprocessor system, as shown in the block diagram. It has these major elements:

### AMBA AHB Master & Slave Wrappers

Enable the core to operate as a master device for data transfers and as a slave device for operations on Special Function Registers (SFRs).

### DMA CTRL & CONV

DMA CTRL is a unidirectional DMA controller that takes pixel data from the AHB Master wrapper (and generates data in test-mode without any AHB bus activity). The CONV module converts incoming pixel data in any of the accepted formats to the standard format, and stores the data in the FIFO buffer.

### FIFO

Buffers the pixel data between the CONV unit and the TV unit. It also works in two clock domains. Its size is parameterized for easy cooperation with off-chip dual-port memory.

### TV

The TV component is a fully configurable display controller, adapted to handle the Analog Devices ADV7174/79 PAL/NTSC video encoder or a similar device. It outputs data in BT.656 8-bit parallel format with horizontal sync (HSYNC), vertical sync (VSYNC) and video blanking (BLANK) signals.

### CONTROL

Eight Special Function Registers (SFRs) and a software reset generation unit, designed to set the required configuration of the core.

## Implementation Results

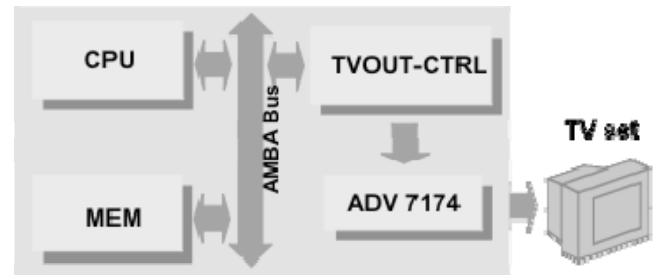
TVOUT-CTRL reference designs have been evaluated in a variety of technologies. The following are sample ASIC results.

Device	Optimized for	Area	Speed
UMC 0.18 $\mu\text{m}$	speed	15,200 gates	200 MHz
UMC 0.18 $\mu\text{m}$	area	14,300 gates	100 MHz

Pixel Clock is fixed at 27 MHz

## Example Application

This example application transmits data from the host memory to the television set. A microcontroller configures the core and processes interrupt requests using the AMBA™ AHB Slave bus. Data from the host memory is sent to the core through the AMBA™ AHB Master interface. The core converts the data and transfers it to an ADV7174 video encoder in YCbCr format, which in turn generates a broadcast signal for the TV.



## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The TVOUT-CTRL core's functionality was verified by processing bitmap pictures. Bitmap files were converted by a "C" program to stimulus and reference files. The stimulus files were applied to core inputs, while the reference files were compared with the core's simulation outputs.

The core has been verified through extensive simulation and rigorous code coverage measurements.

## Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- An example chip implementation, which uses the TVOUT-CTRL in a sample system
- Sophisticated HDL Testbench including external Dual RAM buffers and models of interfaces
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script
- Comprehensive user documentation, including detailed specifications, a system integration guide and a test plan.