

# CAST



## TVOUT-CTRL

### Video Display Controller Core

A semiconductor IP core that implements a video display converter producing standard video data and control signals ready for further processing by an NTSC or PAL broadcast signal encoder. The video data the core produces conforms to the ITU-R BT.601/BT.656 recommendation (formerly CCIR-601 and CCIR-656).

The video display core accepts three different input formats and produces standard 4:2:2 YCbCr pixel data. It also generates all the horizontal and vertical timing periods required for broadcast: horizontal and vertical front porch, back porch, and sync intervals. The core's output signals are compatible with the popular Analog Devices' ADV7174/79 or similar NTSC/PAL video encoder chip.

Ready for easy integration with AMBA-based microprocessor systems, the TVOUT-CTRL includes a wrapper that efficiently interfaces the core DMA, FIFO, and control logic functions with the AMBA High-Speed Bus (AHB).

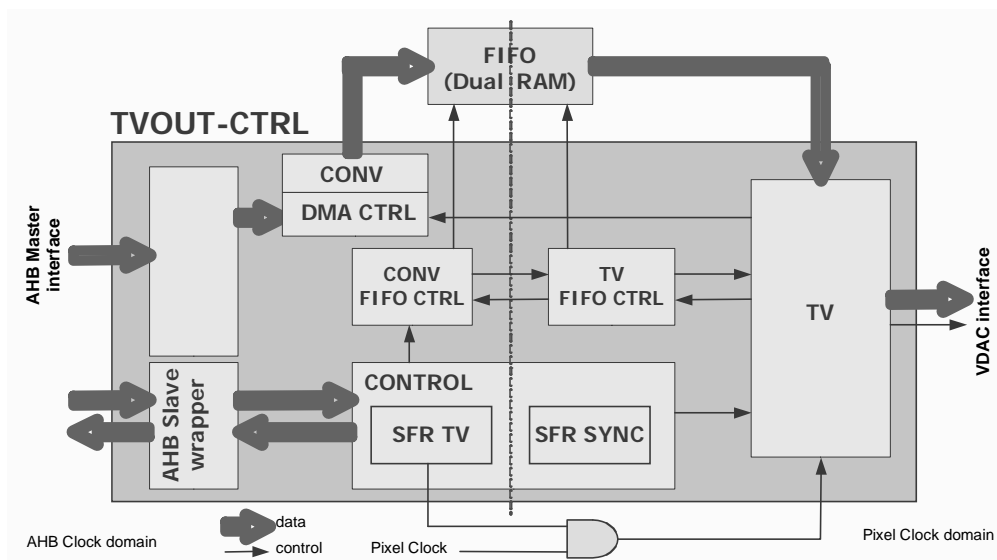
The core is designed for efficient implementation, good performance, and straightforward testing in an ASIC or FPGA SoC design. Typical ASIC results (0.18  $\mu\text{m}$ ) show it to require from 14,300 gates for 100 MHz speed to 15,200 gates for 200 MHz.

### Applications

The TVOUT-CTRL is ideal for use in conjunction with a video data encoder such as the Analog Devices' ADV7174/79 PAL/NTSC video encoder chip. Typical applications include:

- portable video systems
- digital cameras with video output
- advanced mobile phones with video capabilities

### Block Diagram



### Features

- Produces video data that meets the ITU-R BT.601/BT.656 recommendation (without the SAV and EAV features)
- Accepts display data input in three formats:
  - RGB 24 bits/pixel
  - RGB 15 bits/pixel
  - 4:2:2 YUV (YCbCr)
- Provides a video data analog converter (VDAC) interface compatible with an Analog Devices ADV7174/79 chip or similar for PAL/NTSC video signal generation
- Dedicated unidirectional DMA controller with burst transaction support
- Configurable internal FIFO
- Produces 4:2:2 YUV (YCbCr) parallel output format
- Power Save Mode
- Internal, event stimulated, and interrupt request generation, with masking capability
- Integrated test mode – core generates color bar without any AHB bus transactions
- Integrated with AMBA bus:
  - AMBA AHB slave unit to interface with the host controller
  - AMBA AHB master unit to interface with the host memory
- Designed for efficient implementation and straightforward testing in ASICs or SoCs

### Configurability

The TVOUT-CTRL core has a set of synthesizable parameters that allow adjusting the core for the user's application:

- DEPTH – defines the depth of the FIFO memory
- RESET\_ACTIVE\_EDGE – defines the active edge of the clock that is sampling the reset signal between the AMBA and TV clock domains

## Functional Description

The core accepts incoming data from the 32-bit AHB bus in three common video formats: RGB 24 bits per pixel, RGB 15 bits per pixel and 4:2:2 YCbCr. It converts the video data and generates an 8-bit 4:2:2 YCbCr data stream plus all the required control signals. These include horizontal and vertical synchronization signals, and the video blanking signal.

The core interfaces its video data conversion functions with an AMBA AHB-based microprocessor system, as shown in the block diagram. It has these major elements:

### AMBA AHB Master & Slave Wrappers

Enable the core to operate as a master device for data transfers and as a slave device for operations on Special Function Registers (SFRs).

### DMA CTRL & CONV

DMA CTRL is a unidirectional DMA controller that takes pixel data from the AHB Master wrapper (and generates data in test-mode without any AHB bus activity). The CONV module converts incoming pixel data in any of the accepted formats to the standard format, and stores the data in the FIFO buffer.

### FIFO

Buffers the pixel data between the CONV unit and the TV unit. It also works in two clock domains. Its size is parameterized for easy cooperation with off-chip dual-port memory.

### TV

The TV component is a fully configurable display controller, adapted to handle the Analog Devices ADV7174/79 PAL/NTSC video encoder or a similar device. It outputs data in BT.656 8-bit parallel format with horizontal sync (HSYNC), vertical sync (VSYNC) and video blanking (BLANK) signals.

### CONTROL

Eight Special Function Registers (SFRs) and a software reset generation unit, designed to set the required configuration of the core.

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

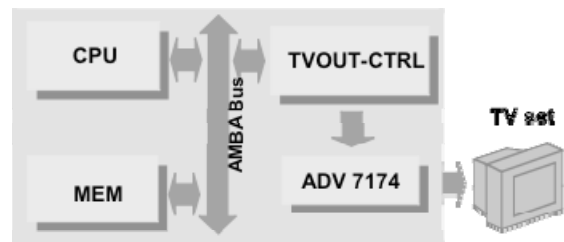
## Implementation Results

TVOUT-CTRL reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results with the pixel clock fixed at 27 MHz. Results for Virtex 4 and Virtex-II Pro use a 512x32-bit dual-port RAM block, and those for Spartan 3 and Spartan 2 use a FIFO with 32-bit-wise data, depth – 9.

Xilinx Device	Area	Speed
Virtex 4 XC4VLX15-12	1214 SLICES 1 RAMBs	112 MHz
Virtex-II Pro XC2VP2-7	1216 SLICES 1 RAMBs	86 MHz
Spartan 3 XC3S400-5	1223 SLICES 1 BRAM	71 MHz
Spartan 2 XC2S100-6	1198 SLICES 4 BRAM	60 MHz

## Example Application

This example application transmits data from the host memory to the television set. A microcontroller configures the core and processes interrupt requests using the AMBA™ AHB Slave bus. Data from the host memory is sent to the core through the AMBA™ AHB Master interface. The core converts the data and transfers it to an ADV7174 video encoder in YCbCr format, which in turn generates a broadcast signal for the TV.



## Verification

The TVOUT-CTRL core's functionality was verified by processing bitmap pictures. Bitmap files were converted by a "C" program to stimulus and reference files. The stimulus files were applied to core inputs, while the reference files were compared with the core's simulation outputs.

The core has been verified through extensive simulation and rigorous code coverage measurements.

## Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- An example chip implementation, which uses the TVOUT-CTRL in a sample system
- Sophisticated HDL Testbench including external Dual RAM buffers and models of interfaces
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications, a system integration guide and a test plan.