

Functional Description

The core combines a flexible data generation module with additional elements necessary to communicate with its host system, accept and convert different forms of video data, and store that data for processing and output.

DMA AHB

Unidirectional DMA controller with an AHB Master Interface. It is implemented to take image data from the AHB data bus. The AHB Master Interface is compatible with the ARM® AMBA™ Advanced High-speed Bus (AHB) interface standard specification version 2.0. It operates as a master device for data transfers, and only read transfers can be initiated. It supports a 32-bit width data bus and a 32-bit width address bus. The AHB Master can initiate only one of the following transfer types: SINGLE, INCR, or INCR16.

AHB Slave

Bidirectional AHB Slave Interface for the CONTROL block. The AHB Slave Interface is compatible with the ARM® AMBA™ Advanced High-speed Bus (AHB) interface standard specification version 2.0. It supports a 32-bit width data bus and a 32-bit width address bus. The AHB Slave supports only SINGLE transfers.

Conv

RGB format converter. Converts input RGB15 format to output RGB24 format and stores into the FIFO.

RGB

Pixel data output and synchronization module. The RGB module takes data from the FIFO and outputs this data with horizontal and vertical synchronization signals (HSYNC and VSYNC), as well as the video blanking signal (Data Enable). Additionally it generates data in test-mode without any AHB bus activity.

SFR Sync

Software reset generation and synchronization module.

Write FIFO CTRL & Read FIFO CTRL

FIFO component implemented in a Dual Port RAM. It is designed to buffer pixel data between the CONV and RGB units and works in two clock domains. The size of the FIFO buffer is parameterized. There are two controllers: WRITE FIFO CTRL for writing data from CONV to FIFO and READ FIFO CTRL for reading data from FIFO to RGB.

The core was designed to make the integration of a high-resolution display controller into an application-specific integrated circuit (ASIC) or a system-on-a-chip (SoC) design easy to accomplish

Implementation Results

DISPLAY-CTRL reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results with a FIFO size of 512x64 bits implemented.

Xilinx Device	Slices	BRAM	I/Os	Fmax (MHz)	ISE
Spartan-3E XC3S1600E-5	1009	2	298	95	12.1i
Spartan-6 XC6SLX75-3	452	2	298	125	12.1i
Virtex-5 XC5VLX50-3	559	1	298	204	12.1i
Virtex-6 XC6SLX75T-3	438	2	298	270	12.1i

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Performance

VESA Monitor Timing Specification contains pixel clock frequencies for standard graphic resolutions; however, the VESA Coordinated Video Timing Generator can be used to calculate reduced timing parameters for LCD panels and monitors. Pixel clock frequency versus on-screen resolution according to VESA CVT is shown in the following table.

Resolution	Refresh Rate	Pixel Clock
320 x 240	85 Hz	8.50 MHz
640 x 480	85 Hz	35.00 MHz
800 x 600	85 Hz	56.75 MHz
1024 x 768	85 Hz	94.50 MHz
1280 x 1024	85 Hz	91.00 MHz
1280 x 720	60 Hz	64.00 MHz
1600 x 1200	60 Hz	130.25 MHz
1920 x 1080	60 Hz	138.50 MHz
1920 x 1200	60 Hz	154.00 MHz

Verification

The core's functionality was verified by processing bitmap pictures. These were converted by a C program into stimuli and reference files. The stimuli files were applied to core inputs, and the reference files compared with the core simulation outputs.

Various resolutions of the core were verified in an AHB bus based system implemented in hardware. Higher resolutions use the Chronitel CH7301C DVI Transmitter up to 165 Mpixels/second.

The DISPLAY-CTRL has also been verified through extensive functional simulation and it has achieved high Code Coverage results. A demo system has been implemented.

Configurability

The DISPLAY-CTRL core has a set of synthesizable parameters that allow adjustment of the core for a particular application:

DEPTH – defines the depth of the FIFO memory

LEVEL_AFULL – defines the almost full level of the FIFO

Default endianness type is Little-endian.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Sophisticated self-checking HDL Testbench including:
 - An example system design
 - External Dual Port TAM
 - Behavioral model of an external Video DAC
 - Example AMBA™ bus systems
 - Clock generator
- Simulation scripts, vectors, and expected results
- Place and route script
- Comprehensive user documentation, including a detailed specification, system integration guide and a verification specification

Related Products

TVOUT-CTRL – is a synthesizable core which implements a video display controller compatible with the ITU-R BT.601/BT.656 recommendation (formally CCIR-601 and CCIR-656). The Video DAC interface of the controller is compatible with Analog Devices' ADV7174/79 encoder video chip. The TVOUT-CTRL accepts three different input formats and produces 4:2:2 YCbCr pixel data format. It can also generate all of the required horizontal and vertical timing periods: horizontal and vertical front porch, back porch and sync intervals.

Application Example

This application enables transmission of data from the host memory to an LCD monitor, or a CRT monitor, or a TFT panel. The CPU controls the configuration of the core and process interrupt requests using an AMBA™ AHB Slave bus. Data from the host memory are sent to the DISPLAY-CTRL through an AMBA™ AHB Master interface. The DISPLAY-CTRL outputs data in RGB24 format. Examples of supported Video DAC devices are:

- ADV7120 – Analog Devices, 80MHz Triple 8-Bit Video DAC
- CH7301C – Chrontel, DVI Transmitter up to 165M pixels/second
- AD9889B – Analog Devices, 165MHz HDMI/DVI Transmitter

ST7787 – Sitronix, 262K Color Single-Chip TFT Controller/Driver

