

# CAST

## DISPLAY-CTRL-4K

### Ultra High Resolution Display Controller Core

Implements a DCI-compatible display controller for ultra-high, 4K resolution graphics displays. Interfaces with microprocessor systems through the AMBA® AXI bus, and provides a complete digital video data path for output to display device interfaces such as DVI or HDMI transmitters.

The Digital Cinema Initiatives compliant display controller supports a wide range of resolutions in both standard and widescreen formats, up to a maximum of 4096 x 2160 pixel resolution video at 24 frames per second with a 36 bit/pixel color depth. It smoothly handles HD video (1920 x 1200) at 60 fps and 48 bits/pixel.

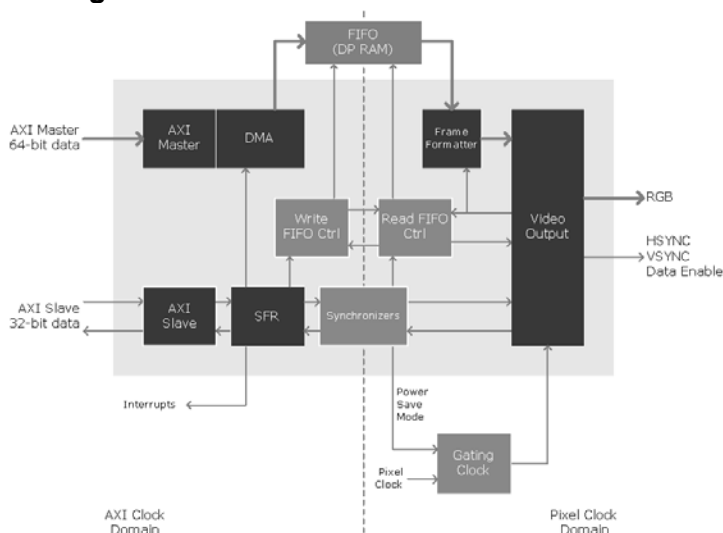
Configurable features help the core work well with a variety of applications and systems. Video data output can be in the popular 24-bit per pixel RGB format, or in other formats such as 30-bits, 36-bits, 48-bits per pixel. The cores features flexible pixel packing over the 64 bit-but data bus of the external memory and internal FIFO and configurable settings for the AXI interface.

### Applications

The core is designed to work with a video data processor in a variety of video display systems, including

- DVI or HDMI transmitter connections
- DisplayPort interface (as the Main Video Stream Source component) connection
- TFT controller (with timing controller) connection
- Standard RGB interface (VGA) with a Video DAC compatible with RS-343A/RS-170 standards connection
- Portable video systems
- Advanced mobile phones with video capabilities

### Block Diagram



### Features

- Maximum supported resolutions:
  - 4096x2160p at 24fps with 36 bits/pixel
  - 1920x1200p at 60fps with 48 bits/pixel
- Video output interface:
  - RGB pixel data (typical 24-bit per pixel)
  - HSYNC and VSYNC signals
  - Data Enable (BLANK) signal
- Progressive scanning mode support
- Fully configurable screen resolutions and aspect ratios
- Configurable polarization of HSYNC and VSYNC signals
- AXI master interface to the system memory:
  - DMA function
  - 64-bit data width
  - Multiple outstanding transactions
  - Long bursts
- AXI slave interface to the host controller:
  - SFR access
  - 32-bit data buses
  - Single transactions
- Configurable internal FIFO
- Internal, event stimulated, interrupt request generation with masking capability
- Integrated test mode – generates color bar without any AXI bus transactions
- Power Save Mode

### Benefits

- Digital Cinema Initiatives (DCI) 4K display compliant
- Configurable screen resolutions according to VESA or CEA standards or specific user requirements.
- All horizontal and vertical timing parameters are programmable via Special Function Registers (SFR)
- Seamless AMBA® AXI bus integration, with support for multiple outstanding transactions and long bursts support
- Glueless connection to any AXI memory controller
- Independent from external memory type, and tolerant to external memory access latency

## Functional Description

The core takes data from system memory and stores it in the FIFO. After formatting a frame, it generates an RGB pixel data stream and the Horizontal and Vertical Synchronization signals as well as the Data Enable signal.

### DMA AXI Master

This unidirectional DMA controller with the AXI Master Interface fetches data from the AXI data bus and puts it into the FIFO. All data transfers from the external memory are performed in a burst mode to better utilize AXI interface bandwidth. The default-configured DMA AXI Master operates with 16-beat burst transfers and can issue up to 16 outstanding addresses. Burst length and read issuing capability are programmable via SFR.

The AXI Master Interface is compatible with the *AMBA AXI Protocol Specification, IHI 0022B, ARM, March 19, 2004*.

### AXI Slave

This bidirectional AXI Slave Interface for the SFR block supports single transfers for 32-bit wide data and address buses. It is compatible with the *AMBA AXI Protocol Specification, IHI 0022B, ARM, March 19, 2004*.

### Frame Formatter

Fetches data from the FIFO, formats data to required the RGB pixel format, and sends it to the Video Output block.

### Video Output Block

This pixel data output and synchronization module takes data from the Frame Formatter and outputs it with Horizontal and Vertical Synchronization signals (HSYNC and VSYNC) and the Data Enable signal (video blanking). It also generates data in test mode without any AXI Master activity.

### SFR Special Function Registers Block

Programs the display controller parameters, mask interrupts, and check display controller status.

### Synchronizers

The synchronization module for Clock Domain Crossing signals.

### FIFO & Write FIFO Ctrl & Read FIFO Ctrl

FIFO memory implemented in a Dual Port RAM. The size of the FIFO memory is parameterized.

There are two FIFO controllers: Write FIFO Ctrl for writing data from DMA to FIFO, and Read FIFO Ctrl for reading data from FIFO to Frame Formatter.

## Configurability

A set of synthesizable parameters allow adjustment of the core for a particular application:

- DATA0M\_WIDTH – defines the width of the AXI Master read data bus
- ADDR0M\_WIDTH – defines the width of the AXI Master address bus

- ADDR0S\_WIDTH – defines the width of the AXI Slave address bus
- ID\_TAG – defines the ID Tag value for the arid0m signal generated by the AXI Master
- DEPTH – defines the depth of the FIFO memory.

## Implementation Results

DISPLAY-CTRL-4K reference designs have been evaluated in a variety of technologies. The following ASIC result is optimized for speed.

ASIC Technology	Approx. Area	Frequency (aclk)	Frequency (clk_pxl)
TSMC 40 nm LP	17,000 gates	450 MHz	450 MHz

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The AXI protocol verification was performed to check if the AXI interfaces of the core meet the specification requirements. Both the AXI Master interface and AXI Slave interfaces were verified. The Mentor Graphics 0-In assertion based tools were used; 100% of assertions were proven.

The functional simulation of the core was performed by a Testbench and ARM AXI Protocol Checkers. The Mentor Graphics QuestaSim tools were used to perform the functional simulation.

Moreover the FPGA validation was performed for following configuration:

- 1920x1080p 60fps 24-bit/pixel and 1920x1200p 60fps 24-bit/pixel
- AXI master port with 64-bit data bus
- 16 outstanding transactions
- FIFO 256 x 64-bit
- DDR2 SDRAM for video data
- DVI interface for LCD monitor

The FPGA validation was performed using Xilinx Virtex-5 FPGA and Xilinx ISE tools.

## Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation.

- Verilog source code (ASIC) or a targeted netlist (FPGA)
- Example design CHIP-DISPLAY-CTRL-4K
- Sophisticated HDL Testbench including external dual port RAM, transactor modules for AXI interfaces, monitor module for video output interface, ARM<sup>®</sup> AXI protocol checkers, and clock generators
- Simulation scripts, vectors, and expected results
- Synthesis (soft) or place and route (firm) script
- Comprehensive user documentation, including a design specification, verification specification, test plan, and integration manual.

## Application Example

The system CPU controls the configuration of the core and processes interrupt requests by using an AMBA<sup>®</sup> AXI Slave bus. Video data from the host memory is sent to the core through an AMBA<sup>®</sup> AXI Master interface. The core outputs pixel data in RGB format.

Examples of supported Video Transmitter or Video DAC devices are:

- CH7301C – Chrontel<sup>®</sup>, DVI Transmitter up to 165M pixels/second
- AD9889B – Analog Devices<sup>®</sup>, 165MHz HDMI/DVI Transmitter
- ST7787 – Sitronix<sup>®</sup>, 262K Color Single-Chip TFT Controller/Driver
- ADV 7120 – Analog Devices<sup>®</sup>, 80MHz Triple 8-Bit Video DAC

This figure shows two applications of the core, enabling transmission of video data from host memory to either an LCD monitor in one or to a TFT panel in the other.

