

CAST



PCIEXPAIF

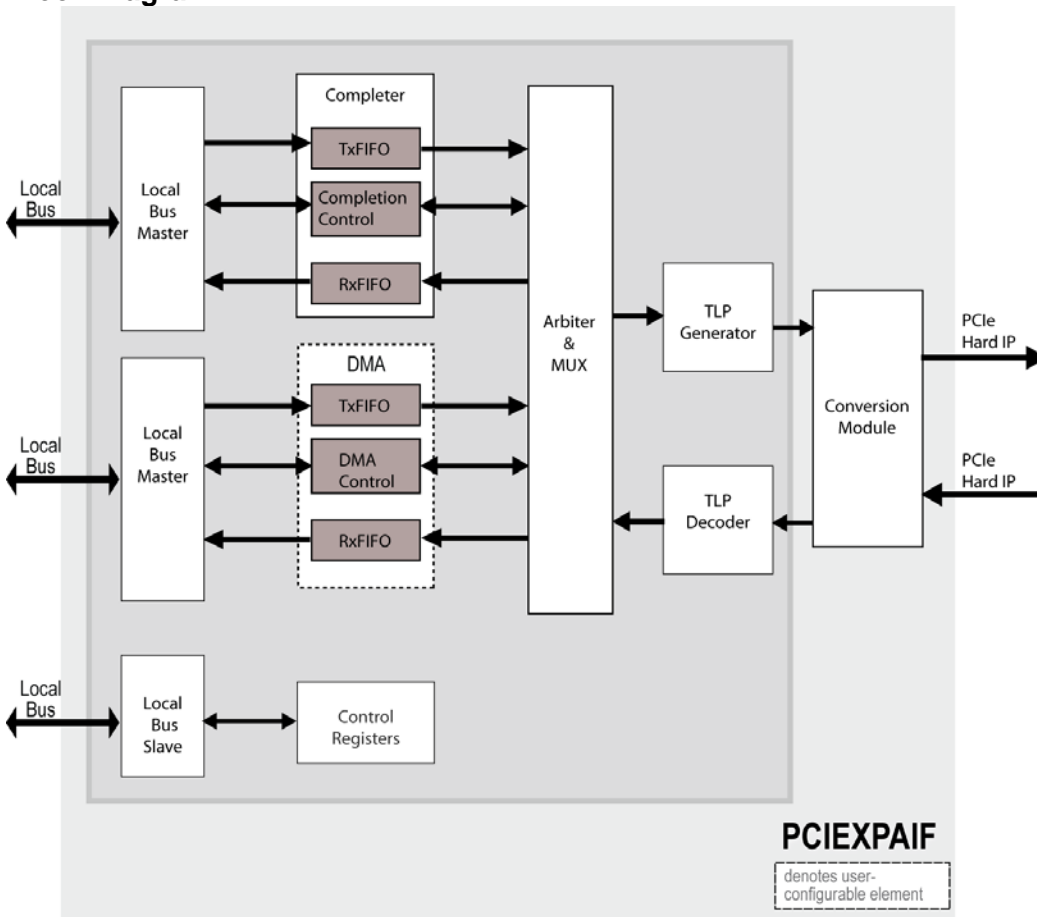
Application Interface
core for Xilinx FPGA
PCIe Hard IP

Implements a PCI Express application-level interface that simplifies the integration of the hard macro PCIe controllers available from Xilinx.

The core integrates a completer controller and DMA controller with up to eight DMA channels. The functionality of the DMA controller can be extended using the Scatter-Gather controller. The Application Interface (AIF) provided by this core is more than a just a DMA core, as it also capable of encoding and decoding for Transaction Layer Packets (TLP). Relieving the SoC designer from the complexity of TLP handling, this core makes integrating PCI Express in a system significantly easier than using other DMA cores for the PCIe Hard IP block.

The PCIEXPAIF core is compatible with Virtex-5, Virtex-6 and Spartan-6 devices. Supported SoC busses are 32bits and 64bits versions of Wishbone, AMBA™ AHB, AXI and AXI4.

Block Diagram



Features

- TLP Encoding/Decoding and Completion Controller for easier system integration
- Flexible DMA
 - Configurable FIFO sizes
 - Up to eight independent DMA channels
 - Optional Scatter-Gather functionality
- Control registers accessible from SoC bus and PCIe bus side
- Interrupt support
- Provides interface to popular system buses:
 - Wishbone bus specification compliant
 - AMBA AHB
 - AMBA AXI
 - AMBA AXI4
- Provides interface to popular system buses:
 - Wishbone bus specification compliant
 - AMBA AHB
 - AMBA AXI
 - AMBA AXI4
- Xilinx version supports these devices:
 - Virtex-5
 - Virtex-6
 - Spartan-6

Functional Description

The core is divided into following main modules:

Conversion module provides interface conversion between PCIe Hard IP block and native CPXP-AIF core.

TLP decoder decodes TLP packets received from the PCIe Hard IP block and provides appropriate data and parameters to the application interface subsystems processing received packet data.

TLP generator generates TLP packets using parameters and data provided by the application interface subsystems. TLP packets are then sent to the PCIe Hard IP block.

Completer responds to memory and I/O read or write requests.

DMA controller performs data transfers between local bus system and a memory located in the PCIe address space. The DMA controller implements up to 8 independent DMA channels.

Implementation Results

PCIEXPAIF example design has been evaluated in Xilinx prototyping boards; the results from several implementations of the core are shown below.

Device	Local bus type	DMA channels	Maximum payload	Slices	BRAM
Virtex-5 XC5VLX50T-1	AXI 32-bit / 62.5MHz	2	256	2053	3
Virtex-5 XC5VLX50T-1	AHB 32-bit / 125MHz	2	256	2072	3
Virtex-5 XC5VLX50T-1	AXI 64-bit / 125MHz	2	256	2356	3
Virtex-6 XC6VLX75T-1	AHB 32-bit / 125MHz	2	256	1800	6
Virtex-6 XC6VLX75T-1	AXI 64-bit / 125MHz	2	256	2268	6
Spartan-6 XC6SLX45T-3	AXI4 32-bit / 62.5MHz	2	256	2231	8

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation. It has also been verified in a prototyping FPGA board platform.

Deliverables

The core is available in synthesizable or netlist forms, and includes everything required for successful implementation:

- HDL RTL source or post-synthesis netlist
- Sophisticated HDL Testbench including models of interfaces, and the core
- Simulation scripts, vectors, expected results
- Place and route scripts
- Comprehensive user documentation

Example Application

