PCIEXPAIF
Application Interface
megafonction for Altera
FPGA PCIe Hard IP

Implements a PCI Express application-level interface that simplifies the integration of
the hard macro PCIe controllers available from Altera.

The megafunction integrates a completer controller and DMA controller with up to eight
DMA channels. The functionality of the DMA controller can be extended using the Scat-
er-Gather controller. The Application Interface (AIF) provided by this megafunction is
more than just a DMA megafunction, as it also capable of encoding and decoding for
Transaction Layer Packets (TLP). Relieving the SoC designer from the complexity of
TLP handling, this megafunction makes integrating PCI Express in a system significant-
ly easier than using other DMA megafunctions for the PCIe Hard IP block.

The PCIEXPAIF megafunction for Altera is compatible with Cyclone IV GX, Arria II GX,
Stratix IV GX, and Stratix V GX devices.

**Block Diagram**

- TLP Encoding/Decoding and Completion Controller for easier system integration
- Flexible DMA
  - Configurable FIFO sizes
  - Up to eight independent DMA channels
  - Optional Scatter-Gather functionality
- Control registers accessible from SoC bus and PCIe bus side
- Interrupt support
- Provides interface to popular system buses:
  - Wishbone bus specification compliant
  - AMBA AHB
  - AMBA AXI
  - AMBA AXI4
- Provides interface to popular system buses:
  - Wishbone bus specification compliant
  - AMBA AHB
  - AMBA AXI
  - AMBA AXI4
- Altera version supports these devices:
  - Cyclone IV G,
  - Arria II GX,
  - Stratix IV GX, and
  - Stratix V GX
**Functional Description**

The megafunction is divided into following main modules:

- **Conversion module** provides interface conversion between PCIe Hard IP block and native CPXP-AIF megafunction.
- **TLP decoder** decodes TLP packets received from the PCIe Hard IP block and provides appropriate data and parameters to the application interface subsystems processing received packet data.
- **TLP generator** generates TLP packets using parameters and data provided by the application interface subsystems. TLP packets are then sent to the PCIe Hard IP block.
- **Completer** responds to memory and I/O read or write requests.
- **DMA controller** performs data transfers between local bus system and a memory located in the PCIe address space. The DMA controller implements up to 8 independent DMA channels.

**Implementation Results**

PCIEXPAIF example design has been evaluated in Altera prototyping boards; the results from several implementations of the megafunction are shown below:

<table>
<thead>
<tr>
<th>Device</th>
<th>Local bus type</th>
<th>DMA channels</th>
<th>Maximum payload</th>
<th>ALM / LC</th>
<th>Memory (bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cyclone IV GX</td>
<td>AXI 32-bit / 62.5MHz</td>
<td>2</td>
<td>256</td>
<td>6262</td>
<td>40128</td>
</tr>
<tr>
<td>Cyclone IV GX</td>
<td>AHB 32-bit / 125MHz</td>
<td>2</td>
<td>256</td>
<td>5761</td>
<td>40128</td>
</tr>
<tr>
<td>Arria II GX</td>
<td>AXI 32-bit / 125MHz</td>
<td>2</td>
<td>256</td>
<td>3157</td>
<td>40128</td>
</tr>
<tr>
<td>Stratix IV GX</td>
<td>AXI 64-bit / 125MHz</td>
<td>2</td>
<td>256</td>
<td>3295</td>
<td>40128</td>
</tr>
<tr>
<td>Stratix V GX</td>
<td>AXI 64-bit / 125MHz</td>
<td>2</td>
<td>256</td>
<td>4562</td>
<td>40128</td>
</tr>
</tbody>
</table>

**Support**

The megafunction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

**Verification**

The megafunction has been verified through extensive simulation. It has also been verified in a prototyping FPGA board platform.

**Deliverables**

The megafunction is available in synthesizable or netlist forms, and includes everything required for successful implementation:

- HDL RTL source or post-synthesis netlist
- Sophisticated HDL Testbench including models of interfaces, and the megafunction
- Simulation scripts, vectors, expected results
- Place and route scripts
- Comprehensive user documentation

**Example Application**