

CAST

CPXP-EP

PCI Express Endpoint Controller Core with SoC Bridge Extensions for AHB, AXI and Wishbone

Implements a PCI Express endpoint controller that is compliant with PCI Express Base specification 1.1, including the Transaction, Data Link, and Physical protocol layers. It is available to act as a bridge to standard buses including AMBA™ AHB, AMBA™ AXI and Wishbone.

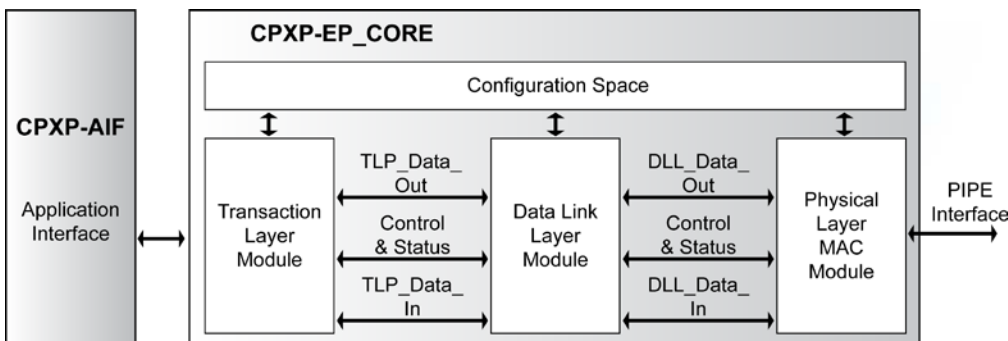
The scalable and flexible core has a modular architecture and a high-performance, low-latency design. It supports multiple device link widths to better match the bandwidth needs of specific applications—x1 (single lane) and x4 (four lane)—and offers bi-directional data rates from 250MB/s (x1) to 1GB/s (x4). It supports most advanced PCI Express capabilities, including message signaled interrupts, multiple virtual channels, advanced error reporting, end-to-end cyclic redundancy check, and power management features. Multi-lane versions of the core support lane reversal and polarity inversion.

The core has an Application Interface (AIF) layer that makes integration significantly easier by relieving the designer from the complexity of transaction layer packet (TLP) handling. This AIF includes a DMA controller and handles the TLP encoding and decoding, and provides an interface to popular system buses, including Wishbone and AMBA™ AHB, AXI, and AXI4.

The external connection interface from the core conforms to the Intel® PIPE specification, ensuring compatibility with any 16-bit PIPE-compliant physical layer (PHY). The core has been successfully used with PHYs from multiple vendors.

The synchronous, latch-free core design was rigorously verified for compliance with the PCI Express specification, and has passed PCI-SIG certification. The core has been tested for interoperability with multiple motherboards using chipsets from various vendors, and is in use by multiple customers.

Block Diagram



Features

- Compliant with PCI Express Base Specification 1.1
- Implements Transaction, Data Link, and Physical protocol layers in hardware
- Supports x1 and x4 link widths
- Offers a data rate of 2.5 Gbps per lane
- Supports up to eight Virtual Channels
- Supports lane reversal and polarity inversion
- PCI Configuration space type 0 header
- MSI capability support
- End-to-end cyclic redundancy code (ECRC) generation and checking support
- Advanced Error Reporting capability support
- Configurable TLP data payload size, from 128B to 4kB
- Configurable size for the Transmit Retry and Receive data buffers
- Modular architecture
- Synchronous design
- 64-bit internal datapath at 125MHz

Integration

- Application Interface (AIF) for easier system integration using industry standard bus interfaces (e.g., Wishbone, AMBA™); handles up to 8 DMA channels
- Conforms to standard PIPE interface for compatibility with any 16-bit PIPE-compliant PHY

Applications

PCI Express is rapidly being adopted for a variety of interconnection applications, including:

- Network server
- Graphics and multimedia
- Communications and mobile products
- Industrial, automotive, and other embedded system

Certification



The x1 and x4 versions of this core have passed the PCI-SIG PCI Express compliance tests, and appear on their Integrators List.

Functional Description

The core is divided into four modules responsible for the Configuration Space, Transaction Layer, Data Link Layer, and Physical Layer MAC.

Configuration Space

Provides a Configuration space register file type 0. In addition to the mandatory functions, numerous extended capabilities are also supported.

Transaction Layer Module

Responsible for the assembly and disassembly of transaction layer packets. The transaction layer supports four address spaces: Configuration space, Memory space, I/O space and Message Space. Power management services are supported.

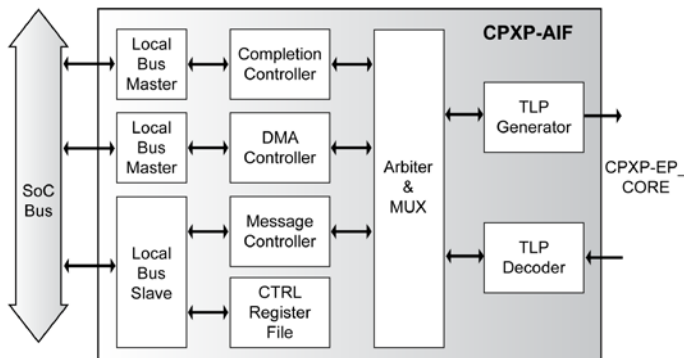
Data Link Layer Module

Responsible for link management, data protection and integrity checking, retry and power management services.

Physical Layer MAC Module

Implements the logical sub-block of the physical layer. The module is responsible for link training and status monitoring, link width negotiation, lane order negotiation, lane polarity reversal control and power management implementation.

SoC Bus Bridge (Application Interface Module)



The SoC Bus bridging feature is added via an additional module called AIF which adds direct SoC bus connectivity with up to 8 DMA channels fully programmable from both the PCIe and SoC busses. The AIF provides a higher-level interface that makes system integration easier than working at the TLP level. The AIF bridge is available for standard SoC busses including AMBA™ AXI, AHB and Wishbone.

The Completion Controller automatically handles read and write requests, and sends completions if needed.

The configurable DMA Controller provides up to eight independent DMA channels.

Implementation Results

CPXP-EP reference designs are being evaluated in a variety of technologies. The following sample results were obtained at the required frequency of 125 MHz, and with a single Virtual Channel (VC0), Maximum Payload of 256B, a 4kB Retry buffer, a 4kB Receive buffer, no ECRC, and using a generic Application Interface.

Link Width	Technology	Approx. Area
x1	TSMC 0.13 μm	45,300 gates
x1	TSMC 0.18 μm	45,100 gates
X1	TSMC 90 nm	41,000 gates
x4	TSMC 0.13 μm	59,300 gates
x4	TSMC 0.18 μm	58,700 gates
x4	TSMC 90 nm	53,800 gates

The core includes an SoC bus bridging module (AIF), an additional subsystem that may be used to integrate the core with SoC designs using custom or various standard interfaces. The sample implementation results shown below show the additional gates needed for a Wishbone AIF with two and eight DMA channels.

DMA Channels	Technology	Approx. Area
2 DMAs	TSMC 0.13 μm	24,400 gates
2 DMAs	TSMC 0.18 μm	23,800 gates
2 DMAs	TSMC 90 nm	21,900 gates
8 DMAs	TSMC 0.13 μm	53,000 gates
8 DMAs	TSMC 0.18 μm	52,400 gates
8 DMAs	TSMC 90 nm	47,000 gates

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has passed PCI-SIG certification and has been verified using Avery's PCI-Xactor verification tool. Interoperability has been verified with Intel, nVidia, VIA, and SIS chipsets, and PHYs from GeneSys Logic, Xilinx, and others have been successfully used by CAST and customers.

Deliverables

The core is available in ASIC (synthesizable) or FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source of the CPXP-EP and CPXP-EP-AIF
- Sophisticated HDL Testbench including external FIFOs, buffers, models of interfaces, and the core
- Simulation script, vectors, and expected results
- Synthesis script; Comprehensive user documentation

See the web site for FPGA version details.