RBBRC

High Performance Raster-to-Block Block-to-Raster Converter Core

Digital image acquisition (display) devices, both static and video, produce (need) image samples on a line-by-line/pixel-by-pixel basis; a scheme well known as raster scan. On the other hand many image processing-transform algorithms work on a block-by-block basis. Typical image processing examples of this kind include types of the N x M image processing filter matrices such as smoothing filters, edge detection filters, noise reduction filters etc. In the image transform context a well known example is the 2D-Discrete cosine transform (2D-DCT), especially the 8x8 block 2D-DCT, found among others in the MPEG video compression and in JPEG image compression.

Streaming applications and applications that cannot afford a full frame buffer but still wish to use such a block-by-block based algorithm face the need of on-the-fly conversion from raster scan pixels to blocks and vice versa. Our RBBRC Raster-to-Block & Block-to-Raster core is designed to be the perfect standalone and on-the-fly conversion solution for the JPEG image compression algorithm. Its use can be extended also to other applications that need to work on rectangle pixel blocks.

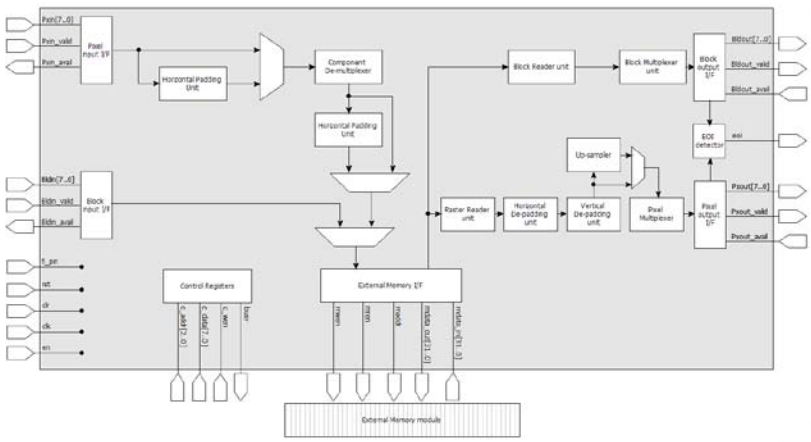
The RBBRC is a microcode-free design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset; therefore scan insertion is straightforward.

Applications

The core is suitable for implementing a wide range of applications, including:

- Image compression / display applications using JPEG codec
- Digital camcorders
- Digital cameras
- Surveillance applications
- Scanners

Block Diagram



Features

- Raster scan to JPEG MCU order
- JPEG MCU order to raster scan
- Full streaming support
- Supported component sampling factors
  - 4:4:4
  - 4:2:2
  - 4:1:1 (horizontal)
  - 4:4:4:4 (CMYK)
  - 1:0:0 (grayscale)
- 8 bit sample precision
- Padding, De-padding
- Up-sampling
- Sustained per cycle operation
- Does not insert extra idle cycles and compensates host stalls – perfect for video encoders and decoders
- High throughput – over 100 MSamples on FPGA platforms
- Standalone operation
- Fully stallable interfaces
- Low power standby mode – global synchronous register enable
- Hardware proven

October 2010

Functional Description

The RBBRC core operates at two distinct modes. The Raster-to-Block operation mode or Forward Operation mode and the Block-to-Raster operation mode or Inverse Operation. The Control Interface is used for programming the operation mode and the conversion-related parameters such as image dimensions, sub-sampling format etc. There is one dedicated interface for each type of data the core accepts or produces, so there are a total of four data I/O interfaces; the Pixel input and block output interfaces that are active during Forward Operation and the Block input and Pixel output interfaces that are active during Inverse Operation. In conjunction with these four interfaces and the control registers interface, there are two more used in both operating modes. These are the external memory interface through which an external memory module that stores conversion intermediate results is accessed and the system interface.

Forward Operation – Raster-to-Block conversion

Core accepts the raster scanned pixels through pixel input interface. Depending on the programmed image dimensions and pixel sub-sampling format, the core, if necessary, performs horizontal image padding by repeating last row sample of each component. Components are then de-multiplexed and, if necessary, vertical padded by repeating last image row for each component. The pixel samples are then stored in the external 16-line double buffer memory. Stored pixels are finally retrieved on a block-by-block basis and they are fed to the block output interface.

Inverse Operation – Block-to-Raster conversion

Core accepts the MCU blocks through block input interface. The MCU interleaved component blocks are de-multiplexed and they are stored to the external double-buffer memory. Then the external memory is addressed in such a way so that image samples are read in raster scan order. According to the programmed image parameters regarding image dimensions and sampling format, the core, if necessary, performs vertical and/or horizontal de-padding at each block of each image component. The component samples are then interleaved according to the image format specified. Finally the interleaved samples are fed to the pixel output interface. If the core is programmed to do so, it will up-sample its output to 4:4:4 format (assuming a 4:2:2 or 4:1:1 input).

Implementation Results

The following are typical performance and utilization results using a variety of implementation technologies.

Asic Silicon Vendor	Technology	Eq. Gates	f_{MAX} (MHz)
UMC	0.18 u	26,000	250
ATMEL	0.18 u	22,000	250

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core includes everything required for successful implementation:

- VHDL or Verilog RTL source code
- Post-Synthesis EDIF (netlist release)
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Simulation and synthesis scripts
- Place & Route scripts (netlist release)
- Documentation & Design Support

CAST
info@cast-inc.com
www.cast-inc.com

CAST, Inc. 11 Stonewall Court
Woodcliff Lake, NJ 07677 USA
tel 201-391-8300 fax 201-391-8694

Alma Technologies
The RBBRC core is sourced from Technology Partner Alma Technologies.