The SPI-MEM-CTRL core offers the interconnection between a host and a serial flash memory using the Serial Peripheral Interface. The SPI-MEM-CTRL supports Single, Dual Input, Dual Input/Output and Quad Input/Output SPI accesses.

The core automatically identifies a variety of serial flash memories and communicates with the attached device at the maximum possible bandwidth. Register accesses are used to insert access requests and read/write data into/out SPI-MEM-CTRL core. Communication with devices other than those automatically identified, is also feasible as the core can be programmed with the memory device parameters. The SPI-MEM-CTRL can read, write or erase any part of the memory.

The core is rigorously verified. A complete verification environment that helps designers verifies the functioning and compliance of the core, and additional aids for system-level simulation are available.

**Applications**

The SPI-MEM-CTRL core is suitable for any SoC design that uses a serial Flash device.

**Block Diagram**
Functional Description

The host introduces the access request and the core begins communication with the serial flash. If the access request is a read then data from the memory is stored on a Read FIFO. The core will inform the host to read out data, once the number of bytes in the Read FIFO becomes larger than a programmable threshold. If the access request is a write, then data to be written in the serial flash memory are stored into a write FIFO. The core will inform the host to write data, once the Write FIFO can accept a number of bytes that is larger than a programmable threshold.

The SPI-MEM-CTRL core is programmed via host interface. When an access request is set, the controller decodes it and sends the serial flash the necessary instructions to serve it. If the access request is a Read the LLSPIC reads data byte by byte using Single/Dual/Quad SPI. Then the data is forwarded in the Read FIFO. The host is signaled when there is enough data in it to take them out. Read access pauses if the Read FIFO gets full. If the access request is a write the LLSPIC sends the data inserted into the Write FIFO to the memory using Single/Dual/Quad SPI. The host is signaled when there is enough empty space in the Write FIFO to insert new data. If the Write FIFO gets empty the write process is paused. If the access request is an Erase the LLSPIC sends the serial flash the appropriate instruction in order to serve the request.

The core can automatically identify which memory is attached among a list of chips supported. The core can be configured during synthesis to add one extra chip with similar behavior to those supported. Furthermore during runtime the host can program the core’s behavior towards the serial flash attached if it is not one of those supported.

Implementation Results

The following are representative ASIC results for the SPI-MEM-CTRL core. Results are optimized for speed, with equivalent NAND2 gate count.

<table>
<thead>
<tr>
<th>ASIC Technology</th>
<th>Number of eq. gates</th>
<th>Fmax (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC 90nm</td>
<td>13,500</td>
<td>&gt; 200</td>
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1. Actual performance is depended on the physical implementation

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The SPI-MEM-CTRL core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- Software (C++) Vector Generator
- Sophisticated HDL Testbench
- Simulation script, vectors and expected results
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide