The SPI-MEM-AXI adds an AMBA™ AXI-4 interface to the Serial Flash Controller (SPI-MEM-CTRL) core. Along with the SPI-MEM-CTRL, this core allows connecting a serial NOR-flash memory device to an AXI-4 SoC bus.

Designed for ease of integration, it integrates two AXI slave interfaces, one for accessing the control and status registers of the SPI-MEM-CTRL, and one for direct memory access through the controller’s Block Read Interface (BRI). The AXI data busses can be 64bit or 32bit wide, and the core takes care of packing and unpacking when the AXI bus width is different than this of the controller native bus.

The core synthesizes to approximately 4,000 gates, and is delivered in RTL source or as targeted FPGA netlist. It has been rigorously verified, and is delivered with a sophisticated test-bench, which includes bus models, and comprehensive documentation.

### Features

**AMBA/AXI-4 wrapper for the Serial Flash Controller Core**
- 32bit or 64bit AXI-4 data busses
- AXI Read/Write Slave interface for control/status register access
- AXI Read Slave interface for direct memory read access
- Pin-compatible with the SPI-MEM-CTRL core
- Runs on AXI bus clock

**High-Quality IP Core**
- Available in RTL or targeted FPGA netlist
- Extensively verified for AMBA/AXI-4 compliance and interoperability with the SPI-MEM-CTRL
- Delivered with a sophisticated test-bench including bus models, scripts and comprehensive documentation

### Block Diagram

![Block Diagram](image)

### Applications

The combination of the SPI-MEM-CTRL and the SPI-MEM-AXI cores is ideal for connecting a microprocessor equipped with an AXI-4 bus to an external serial flash device storing code. The direct random access capability makes it ideal for executing code directly from the flash memory (XIP/execute-in-place) or for copying the code from the serial NOR-flash to an on chip SRAM (shadowing).

### Related Products

SPI-MEM-CTRL: [Serial Flash Memory Controller Core](#)