



SDR-SDRAM-CTRL

Single Data Rate Mobile SDRAM Controller Core

Implements a controller providing a simple, flexible, burst-optimized interface to all industry-standard single data rate (SDR) Mobile and ordinary SDRAM memory devices. Also works with registered/unbuffered DIMMs. It supports up to a 2G (2^{30} word) memory address space, provides up to eight chip selects, and manages up to four memory banks.

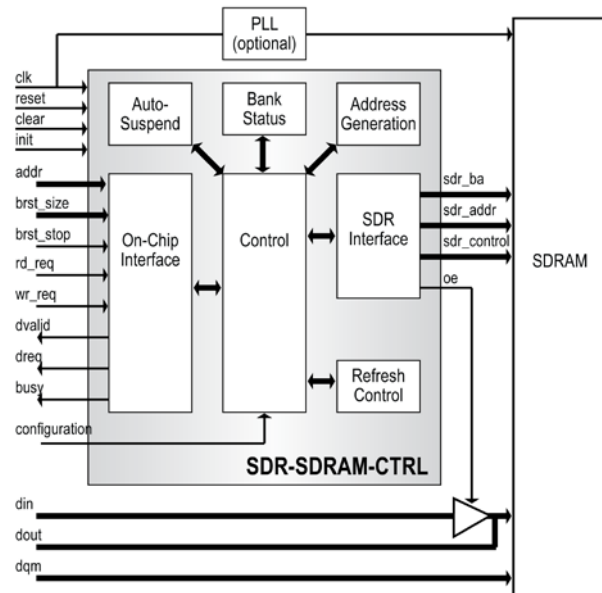
The core automatically handles memory management, initialization, and refresh operations. It gives the user a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing (CAS Latency, tRP, etc.), memory setting (Row Bits, Column Bits, etc.), and Mobile-SD and Extended-Mode-Register settings. A configurable auto-close mechanism precharges inactive memory banks to minimize power dissipation, and configurable power-down and self-refresh features plus support for sleep mode help reduce power consumption.

The flexible user interface features separate read and write ports, and the core handles single word accesses as well as arbitrary-length bursts, emulating a linear memory space with no page or bank boundaries. A pipelined design achieves maximum memory bandwidth utilization, while parallel state machine design practices further improve performance. The rigorously-verified core is silicon-proven and has been embedded in several products. It offers very competitive implementation characteristics, requiring for example just 9,400 gates and running at 200 MHz in a typical .18 micron ASIC process.

Applications

The core's flexibility, performance, and simplicity of use make it an excellent memory controller for nearly any application using the targeted SDRAM and DIMM devices.

Block Diagram



Features

- Interfaces directly to Mobile and ordinary Single Data Rate (SDR) SDRAM chips and registered/unbuffered DIMMS
- Supports address space up to 2G (2^{30} words) and
 - one to eight chip selects,
 - two to four banks,
 - eleven to fourteen row bits,
 - eight to twelve column bits
- Manages up to four 2GB DIMMs
- Automatically generates initialization and refresh sequences
- Efficient bank management and access cascading for up to 100% memory throughput utilization
- Programmable automatic refresh policy reduces refresh overhead
- Runtime-configurable features for application flexibility
 - timing parameters: CAS latency, tRP, tRCD, tRFC, tMRD, etc.
 - memory settings: Row bits, Column bits, Bank bits, number of CSs
 - Mobile-SDR support and Extended-Mode-Register (EMR) values
- Bank status monitoring means banks are opened or closed only when necessary, minimizing access delays
- Configurable auto-close mechanism minimizes power dissipation by precharging inactive banks
- Configurable auto power-down and auto-self-refresh: SDR devices put in power-down mode after some time of inactivity, and in self-refresh mode after a further time of inactivity.
- Energy-saving sleep-mode: after setting SDRAM devices in self-refresh mode, core "turns off" most of the internal circuitry to minimize power dissipation
- Flexible user-interface: separate read and write interfaces support from single to any arbitrary length burst accesses; access lengths defined using an access-size bus and/or a burst-stop signal.
- Easily interfaced to legacy on-chip synchronous microprocessor buses that support burst-accesses and handshaking, or to on-chip FIFOs (respective wrappers available on request)

Functional Description

The core performs all initialization and refresh procedures for the SDRAM to be setup correctly while ensuring the integrity of the data. After the initial delay required by the SDRAM devices has elapsed, the necessary initialization procedure commences depending on the type of SDRAM (mobile or not). Once initialization is complete, the controller can accept read and write requests. The requests are served using a first-come-first-served policy. The controller checks whether the particular memory location can be directly accessed or if bank-precharge and/or bank-activate operations are required. After sending the appropriate command sequences, the controller signals that either valid data exists on the dout-bus or data is required on the din-bus. The pipelined architecture enables the required precharge/activate operations to be issued while performing reads or writes. The core can be configured to automatically precharge activated banks after some time of inactivity, in this case the respective pre-charge commands are performed without obstructing ongoing read/write processes.

The controller has an automatic power-down and suspend mechanism, which puts the SDRAM device into power-down mode after a programmable time of inactivity. If a read/write request is issued, the controller “wakes-up” right away and serves the request. The controller also wakes-up to serve an internal auto-refresh request and then returns to power-down mode. After an additional time of inactivity, the controller enters into suspend mode, where the SDRAM device is put into self-refresh mode and most of the internal circuitry is frozen. When a read or write request is issued, the controller performs the required steps for the device to exit the self-refresh mode and then serves the request.

The controller provides run-time configuration inputs for controlling many SDRAM parameters, including: burst-length, timing parameters, address settings (number of row-bits, column bits, etc.), mobile support, mobile EMR values, etc. This ensures compatibility with virtually any SDRAM device on the market.

Implementation Results

The core has been evaluated in a variety of technologies. The following are sample Xilinx results for a full-featured controller supporting two chip selects, obtained after speed optimization during synthesis and place and route, while assuming that all core I/Os are routed off-chip. (See ASIC results on the web site.)

Xilinx Device	Slices	I/O	Other	Frequency	ISE
Spartan-3 xc3s200-5	628 Slices	155	1 DCM	133 MHz	8.1.03i
Spartan-3E xc3s250e-5	719 Slices	155	1 DCM	150 MHz	8.1.03i
Spartan-6 xc6lx16-2	343 Slices	155	1 DCM	142 MHz ¹	9.1i
Virtex-2 xc2v250-6	634 Slices	155	1 DCM	> 200 MHz	8.1.03i
Virtex--2 Pro xc2vp4-7	622 Slices	155	1 DCM	> 200 MHz	8.1.03i
Virtex--4 xc4vlx15-12	626 Slices	155	1 DCM	> 200 MHz	8.1.03i

Note that the controller core can achieve operating frequencies in excess of 200 MHz with some technologies. However careful clock distribution is essential to support SDRAM devices operating at frequencies higher than 100 MHz. The use of a PLL and/or a clock delay line is required in most cases in order to achieve maximum SDRAM frequencies.

¹ Results not optimized for speed.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation, rigorous code coverage measurements, and FPGA prototyping.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001) and vector generation application
- Simulation script, vectors and expected results
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide

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