

# CAST



## SDIO-HOST

### SD/SDIO/MMC/e-MMC Card Host Controller Core

This IP core implements a host controller that manages communication for SD, MMC, and e-MMC memory cards and SDIO devices connected to a generic or various standard system buses.

Conforming to the latest specifications, the core supports transfer speeds up to 104 MB/sec and capacities up to 2 TB (SDXC cards). A simple 8/16/32-bit master/slave system interface is standard; AMBA/AHB, Avalon, PLB and OCP bus interfaces are available. An OS-independent software driver is also available.

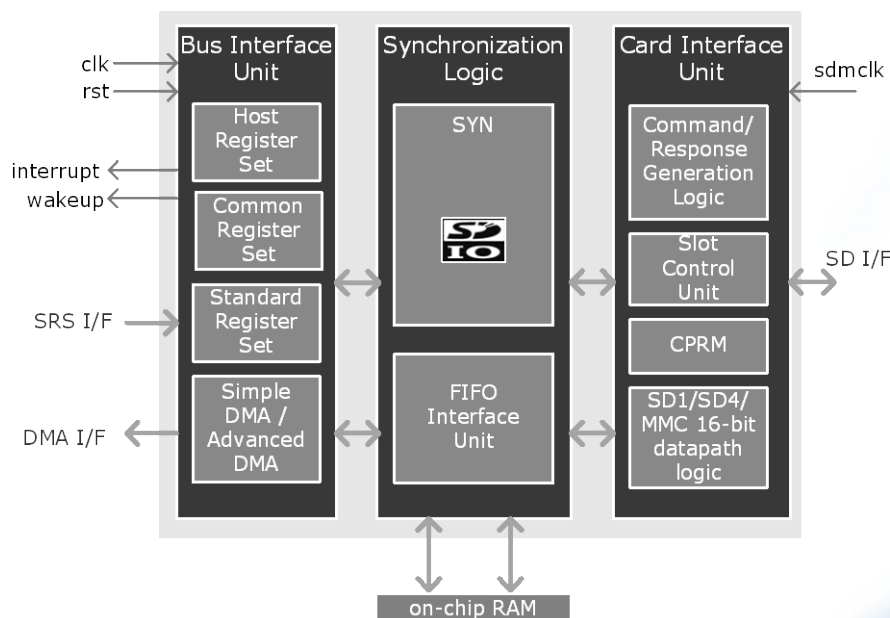
The configurable, multi-slot architecture supports one to four cards, and each can be individually controlled through the Standard Register Set. An optional integrated DMA controller can help offload the system CPU, or be omitted to save silicon area. Content protection features can be included or not, and the core employs various optional power-saving techniques.

The core is competitive in its use of silicon space, requiring under 1.3K Virtex6 slices for a simple single-slot configuration without DMA, or 3.5K Virtex 6 slices for a 4-slot version with Advanced DMA. The rigorously-verified design builds on a previous version that has been production proven multiple times.

### Applications

The SDIO-HOST controller core can be utilized for a variety of applications, including: handheld devices such as digital cameras, camcorders, digital audio players, GPS receivers, cellular phones, and PDAs; consumer electronics including USB SDIO dongles and sensors; and SoC design elements such as wireless modems, digital TV tuners, and fingerprint recognition cards.

### Block Diagram



### Features

- Compliant with latest specs
  - SD Memory Card 3.00 (SD, SDHC, and SDXC cards)
  - SD Host & SDIO Card 3.00
  - MMC and Embedded MMC (e-MMC) Card 4.41
- Broad compatibility
  - Card slots with 1-bit, 4-bit, 8-bit (MMC only) data interface
  - SD cards with UHS-I interface compliant
  - Single Data Rate and Dual Data Rate modes
  - Sample clock tuning logic
  - Signaling level voltage switch
- Multislot operation
  - Supports 1-4 cards/slots with independent clock for each
  - Shared data path (including DMA and FIFO) reduces area
- Optional integrated DMA controller reduces CPU load
  - SDMA (Simple DMA) mode
  - ADMA (Advanced DMA) mode with descriptor-based architecture and arbitrary data buffer alignment
  - No DMA for smallest area
- Flexible data management
  - Configurable 32-bit FIFO buffers (512B - 2kB)
  - Dual-Buffer mode optimizes throughput
- Master/slave system bus interface choices
  - Avalon
  - OCP
  - AMBA AHB
  - PLB
- Independent Interrupt and Wakeup outputs
- Optional CPRM (Content Protection for Recordable Media)
  - Cryptomeria Cipher C2 hardware implementation
  - AKE (Authentication and Key Exchange)
- Low power features
  - Master SD card side clock can be switched off
  - Each card clock can be switched off independently
  - DP RAM can be replaced by SP RAM to reduce power
- OS-independent software driver
- Evaluation Board available

## Functional Description

The SDIO Host Controller core consists of several blocks as shown in the diagram and described below.

### BIU – Bus Interface Unit

Communicates with the host CPU (uses clk system clock domain). The Standard Register Set (SRS) slave interface provides the access to the internal register spaces, including Slot Register Set (SRS), Common Register Set (CRS), and proprietary Host Register Set (HRS). The DMA master interface can be omitted, or used in Simple DMA (SDMA) or Advanced DMA (ADMA) mode.

### CIU – Card Interface Unit

Communicates with the SD/SDIO/MMC cards via the SD bus interface (uses sdmcclk clock domain). It contains card clock dividers, Command/Response generation logic (CMD), and SD1/SD4/MMC 16-bit datapath logic (DAT). Most components are shared among all slots to reduce the area. Independent components for each slot are grouped in a Slot Control Unit (SCU). The optional CPRM module enables content encryption.

### FIU – FIFO Interface Unit

Data buffer control logic for data transactions. Two virtual buffers can be loaded inside the on-chip RAM, one dedicated to the BIU side, the other can simultaneously be accessed by the CIU ("dual-buffer" mode). The actual memory is outside the core on the chip level. Dual-Port (DP) RAM memory can be used to achieve high performance (by enabling dual-buffer mode), or Single-Port (SP) RAM for lower power consumption and less silicon area (working in single-buffer mode only).

### SYN – Synchronization Logic

Cross clock domain synchronization for all control paths.

## Support

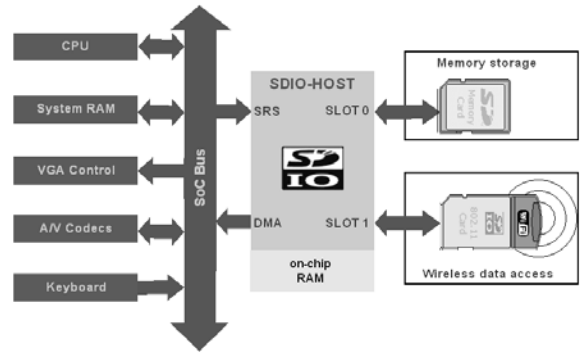
The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

## Example Application

This smartphone example design uses one slot of the SDIO-HOST controller for access to external SD memory cards, and a second slot to communicate with a wireless SDIO modem card. The software running on the CPU can implement applications such as a media player, a text processor, as well as a web browser and an e-mail client.



## Implementation Results

SDIO-HOST reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results for the core configured with, FIFO buffer size of 2 \* 2kB, a 32-bit Generic interface, memories, and no CPRM.

Family	Slice	BRAM	Fmax (MHz)	Config.
Virtex5 xc5vfx70t-3	1508	1 RAM36K	208	No DMA, 1 Slot,
Virtex6 xc5vfx70t-3	1281	1 RAMB36E1	208	
Spartan6 xc6slx100t-4	1399	2 RAMB16BW	100	
Virtex5 xc5vfx70t-3	1784	1 RAM36K	208	Simple DMA, 1 Slot,
Virtex6 xc5vfx70t-3	1623	1 RAMB36E1	208	
Spartan6 xc6slx100t-4	1617	2 RAMB16BW	100	
Virtex5 xc5vfx70t-3	2210	1 RAM36K	208	Advanced DMA, 1 Slot
Virtex6 xc5vfx70t-3	2020	1 RAMB36E1	208	
Spartan6 xc6slx100t-4	2223	2 RAMB16BW	100	
Virtex5 xc5vfx70t-3	3918	1 RAM36K	208	Advanced DMA, 4 Slots
Virtex6 xc5vfx70t-3	3468	1 RAMB36E1	208	
Spartan6 xc6slx100t-4	3764	2 RAMB16BW	100	

## Deliverables

The core includes everything required for implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Example implementation illustrating how to build and connect memories and tristate buffers
- Sophisticated HDL Testbench including external FIFOs, buffers, models of interfaces, and the core
- Simulation and Place and route scripts
- Comprehensive user documentation