



# SDIO-HOST

## SD/SDIO/MMC/e-MMC Card Host Controller Megafunction

This IP megafunction implements a host controller that manages communication for SD, MMC, and e-MMC memory cards and SDIO devices connected to a generic or various standard system buses.

Conforming to the latest specifications, the megafunction supports transfer speeds up to 104 MB/sec and capacities up to 2 TB (SDXC cards). A simple 8/16/32-bit master/slave system interface is standard; AMBA and OCP bus interfaces are available. An OS-independent software driver is also available.

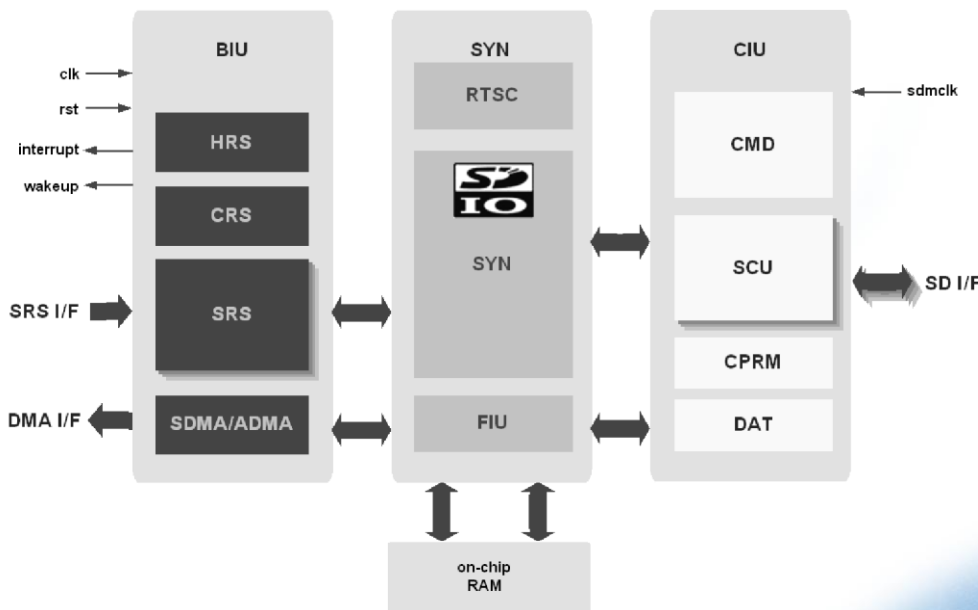
The configurable, multi-slot architecture supports one to four cards, and each can be individually controlled through the Standard Register Set. An optional integrated DMA controller can help offload the system CPU, or be omitted to save silicon area. Content protection features can be included or not, and the megafunction employs various optional power-saving techniques including the use of Single-Port versus Dual-Port RAM.

The megafunction is competitive in its use of silicon space, requiring under 33K gates for a simple single-slot configuration without DMA, or 69K gates for a 4-slot version with Advanced DMA. The rigorously-verified design builds on a previous version that has been successfully implemented by multiple customers.

### Applications

The SDIO-HOST controller megafunction can be utilized for a variety of applications, including: handheld devices such as digital cameras, camcorders, digital audio players, GPS receivers, cellular phones, and PDAs; consumer electronics including USB SDIO dongles and sensors; and SoC design elements such as wireless modems, digital TV tuners, and fingerprint recognition cards.

### Block Diagram



### Features

- Compliant with latest specs
  - SD Memory Card 3.00 (SD, SDHC, and SDXC cards)
  - SDIO Card 2.00
  - MMC and Embedded MMC (e-MMC) Card 4.4
  - SD Host 2.00 part A2
- Broad compatibility
  - 1-bit, 4-bit, 8-bit (MMC only) DAT bus width
  - SD cards with UHS-I interface compliant
  - Single Data Rate and Dual Data Rate modes
- Multislot operation
  - Supports 1-4 cards/slots with independent clock for each
  - Shared data path (including DMA and FIFO) reduces area
- Optional integrated DMA controller reduces CPU load
  - SDMA (Simple DMA) mode
  - ADMA (Advanced DMA) mode with descriptor-based architecture and arbitrary data buffer alignment
  - No DMA (register access only) for smallest area
- Flexible data management
  - Configurable 32-bit FIFO buffers (512B - 2kB)
  - Dual-Buffer mode optimizes throughput
  - Dual-Port or Single-Port RAM
- Master/slave system bus interface choices
  - 8/16/32-bit Generic Interface
  - 8/16/32-bit OCP Interface
  - 32-bit AMBA AHB™ Interface
- Independent Interrupt and Wakeup outputs
- Optional CPRM (Content Protection for Recordable Media)
  - Cryptomeria Cipher C2 hardware implementation
  - AKE (Authentication and Key Exchange)
- Low power features
  - Master SD card side clock can be switched off
  - Each card clock can be switched off independently
  - DP RAM can be replaced by SP RAM to reduce power
- Software driver available (operating system independent)
- Evaluation Board available

## Functional Description

The SDIO Host Controller megafunction consists of several blocks as shown in the diagram and described below.

### BIU – Bus Interface Unit

Communicates with the host CPU (uses clk system clock domain). The Standard Register Set (SRS) slave interface provides the access to the internal register spaces, including Slot Register Set (SRS), Common Register Set (CRS), and proprietary Host Register Set (HRS). The DMA master interface can be omitted, or used in Simple DMA (SDMA) or Advanced DMA (ADMA) mode.

### CIU – Card Interface Unit

Communicates with the SD/SDIO/MMC cards via the SD bus interface (uses sdmclock clock domain). It contains card clock dividers, Command/Response generation logic (CMD), and SD1/SD4/MMC 16-bit datapath logic (DAT). Most components are shared among all slots to reduce the area. Independent components for each slot are grouped in a Slot Control Unit (SCU). The optional CPRM module enables content encryption.

### FIU – FIFO Interface Unit

Data buffer control logic for data transactions. Two virtual buffers can be loaded inside the on-chip RAM, one dedicated to the BIU side, the other can simultaneously be accessed by the CIU ("dual-buffer" mode). The actual memory is outside the megafunction on the chip level. Dual-Port (DP) RAM memory can be used to achieve high performance (by enabling dual-buffer mode), or Single-Port (SP) RAM for lower power consumption and less silicon area (working in single-buffer mode only).

### SYN – Synchronization Logic

Cross clock domain synchronization for all control paths.

### RSTC – Reset Controller

Generates a reset signal for every internal block using any of four triggers: hardware reset, software reset for all (clears all flip-flops except card detection logic), software reset for CMD (clears command/response logic), or software reset for DAT (clears the datapath logic).

## Support

The megafunction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The megafunction has been verified through extensive simulation and rigorous code coverage measurements.

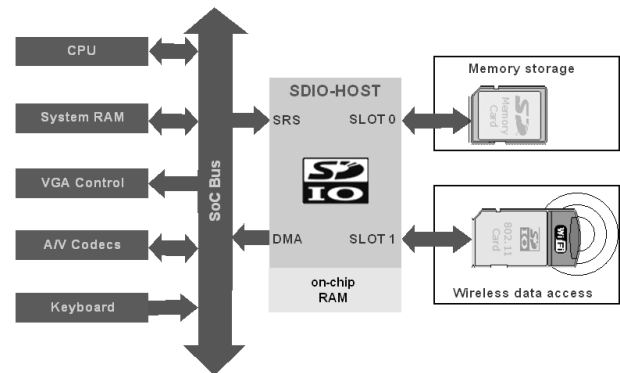
## Implementation Results

SDIO-HOST reference designs have been evaluated in a variety of technologies. The following are sample Altera results using a FIFO buffer size of 2 \* 2kB, a 32-bit Generic interface, memories, and no CPRM.

Altera Technology	Area/Speed			
	1 slot, no DMA	2 slots, SDMA	1 slot, SDMA+ADMA	4 slots, SDMA+ADMA
Cyclone-III EP3C16-6		8051LEs 4 M9Ks / 136 MHz		
Cyclone-IV EP4CGX30-6		71015 LEs 4 M9Ks / 161 MHz		
Stratix III EP3S50-3	3201 ALUTs 5 M9Ks / 200 MHz		5223 ALUTs 5 M9Ks / 145MHz	7056 ALUTs 8 M9Ks / 145MHz
Stratix-IV EP4SGX70-2		4552 ALUTs 4 M9Ks / 208 MHz		

## Example Application

This Personal Digital Assistant (PDA) design uses one slot of the SDIO-HOST controller for access to external SD memory cards, and a second slot to communicate with a wireless SDIO modem card.



## Deliverables

The megafunction includes everything required for implementation. The Altera version includes:

- Post-synthesis EDIF netlist
- Example implementation illustrating how to build and connect memories and tristate buffers
- Sophisticated HDL Testbench including external FIFOs, buffers, models of interfaces, and the megafunction
- Simulation script and macros
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide