PFLASH-CTRL
Parallel NOR Flash Controller Core

This memory controller core is a configurable module designed to interface an AMBA AHB bus to an external, parallel NOR Flash memory device. It bridges a 32-bit AHB system bus to a generic external bus that can be connected to almost any parallel NOR Flash device.

Designed for ease of use, the memory controller core allows word, half-word, and byte width addressing to 32-bit, 16-bit, and 8-bit Flash devices. Also, the number of read and write wait-states and the memory size are configurable to allow proper communication with different Flash devices. Software drivers and modified interfaces are available on request. Support for the AMBA AXI protocol is available as an option. The PFLASH-CTRL core is production proven and available in RTL source or as a targeted FPGA netlist.

Applications
This NOR Flash controller core is ideal for connecting a microprocessor equipped with an AHB bus to an external parallel NOR Flash device storing program execution code. The direct random access capability makes it ideal for executing code directly from the flash memory (XIP/execute-in-place) or for copying the code from the serial NOR Flash to an on-chip SRAM (shadowing).

Support
The PFLASH-CTRL as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Block Diagram