



NANDFLASH-CTRL

NAND Flash Memory Controller Megafunction

Implements a flexible ONFI 2.2 compliant controller for NAND flash memory devices from 2 Gb and higher (single device).

The full-featured core efficiently manages the read/write interactions between a master host system and Single- or Multi-Level Cell (SLC or MLC) NAND flash memory devices. The core includes an optional direct memory access (DMA) manager, uses a comprehensive command set for easy NAND Flash memory access, automatically remaps corrupted memory blocks to improve reliability, can protect memory areas against writes with a block lock mode, has built-in power-saving features, and can boot software directly from Flash memory.

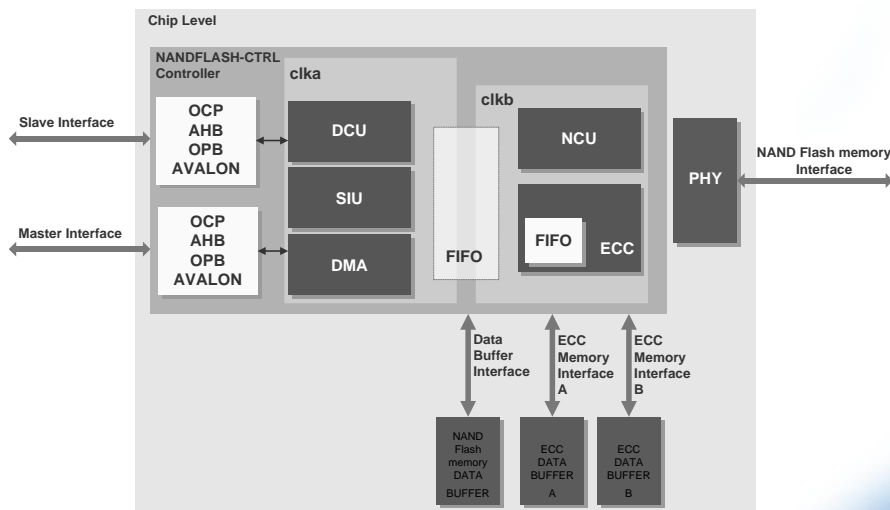
The controller works with any suitable memory device with 512 Bytes to 32-kB page sizes supporting the Open NAND Flash Interface Working Group (ONFI) standards.

The NAND Flash Controller employs a standard OCP 2.0 socket interface to facilitate easy adaption into all types of design structures depending on the designer needs. OCP is being widely adopted due to its ease of integration and flexibility. Wrappers supporting AMBA 2 AHB, OPB/PLB, Avalon and FlexBus buses are available and other structures are available by request.

The Controller offers two error code correction (ECC) mechanisms from the relatively simple single-bit Hamming Code to more sophisticated high-speed BCH (Bose, Ray-Chaudhuri and Hocquenghem) ECC. BCH targets applications with high-density memory as well as direct boot from the NAND flash device.

This fourth-generation product builds on silicon-proven previous versions of the controller. Developed for reuse in ASICs and FPGAs, the core is fully synchronous with positive-edge clocking, has no internal three-state buses, and uses a synchronous reset so scan insertion is straightforward. The included verification package features bus models for the AHB master and NAND flash devices to help designers verify the functioning of the core.

Block Diagram



Features

- Support for High Speed NAND Flash memories (up to 200MB/s)
- Command interface conforms to ONFI Standard 1.x & 2.2 for compatibility with major manufacturers (e.g., Micron, Numonyx)
- Support for popular standard memory device manufacturers (e.g. Samsung, Toshiba, etc.)
- Supports Single- and Multi-Level Cell (SLC and MLC) flash devices from 2 Gb to 32Gb for SLC and higher for MLC
- Two options for ECC:
 - Simple Hamming-Code mechanism (for SLC devices)
 - Sophisticated BCH multiple-bit mechanism (for MLC devices) correcting up to 32 bits
- Supports page sizes from 512 Bytes to 32 kB
- OCP 2.0 socket interface for easy integration with any system bus
- Available system interfaces wrapper supports:
 - AMBA™ AHB
 - OPB/PLB
 - Avalon
 - FlexBus
- Custom development of system bus wrappers
- Configurable number of memory banks and devices per bank
 - Define number of chip select, ready/busy, and write protect signals
 - Allows different memory type for each bank
- Enables booting from flash, with configurable boot sequence
- Adapts to a variety of system and memory types, with configurable (via special function registers):
 - timing parameters
 - 4/5 address cycles
 - ECC calculation turn on/off
 - Write/Erase Protection size
 - Interrupt enable/disable
 - Built-in optional Direct Memory Access (DMA) manager to speed data transfer and off-load the host

Features (Continued)

- Synchronous (DDR mode) and asynchronous interfaces
- Bad Block management supports Automatic Write/Read Page (with data correction)
- Extended Power Save Mode for low-power applications
- Optional support for the Write/Erase Protection
- Easily adjustable generic parameters
 - Number of device banks
 - Endian Type (Big or Little)
- Custom NAND Flash Controller Driver available; allows designer to develop system software without detailed NAND flash controller knowledge

Applications

The core is suitable for controlling embedded storage (e.g. in mobile devices, network routers, and point-of-sale systems) and solid state device (SSD) mass storage for USB flash drives, digital cameras, laptops, and more.

NAND Flash Controller Software Driver

- Written in "C"
- Contains functions which support common memory functions
- Contains functions which support custom memory features of Micron, Samsung and ST devices
- DMA support module configures DMA and transmits data
- Configurable to reduce resource requirements
- Hardware mapping of memory blocks
- See associated datasheet

Functional Description

The NANDFLASH-CTRL core is partitioned into modules and comes with external elements as shown in the block diagram and described below.

DCU

The Design Control Unit controls all other modules based on the SFR values and current controller state. The main tasks of this module are:

- Provide enable/disable signal to the DMA and SIU units when they try to get access the FIFO module. Only one of the two units can be active at time.
- Enable/Disable the ECC module.
- Provide control signals to the NCU unit
- Execute the boot sequence
- Interrupt controller

SIU

Opens a window in the address space where the BUFFER and all SFRs are visible, providing access to these elements. Works as glue logic between the system interface and internal controller bus, coordinating their interaction. It is responsible for generating the internal request signal if the controller buffer must be read directly using the

controller interface, and it holds transmission on the external bus if access can't be granted.

DMA

Speeds up data transfer between a device on the system bus and the memory, and decreases system bus burden.

FIFO

A 32-bit width asynchronous FIFO module which facilitates transferring data between the input module and NCU when the command sequence is executed.

NCU

The NAND Control Unit is responsible for generation of the NAND flash device access sequences. The unit uses the control signals provided by the DCU. In some configurations it can be multiple instantiated to allow parallel access to multiple NAND flash devices. The NCU uses our proprietary interface to the PHY Interface unit.

ECC

This is an error correction code calculator and a correction unit. A correction word is calculated for each 512B sub page of the NAND Flash memory page. During the read operation the unit can automatically correct bad bits without any interaction with the external system. It has a status register, the bits of which signal errors occurring during a read, and then inform if errors were corrected. It is possible to choose between a simpler unit that can correct only one error per 512B sub page and a more advanced unit that can correct multiple errors. The choice depends on the NAND Flash memory type that is in use. Depending on the end-user application, it is possible to choose between two solutions. The first one is based on the Hamming algorithm that allows correction of one error for each 512B sub page, which is a good choice for SLC memories. The other solution uses the BCH algorithms and is more efficient if MLC memories are used. The ECC module has an integrated FIFO that is used to transfer the calculated words to the NCU modules during the encode process, and to store the calculated partial syndromes during the decode process.

PHY

This module provides the DDR data interface for the new High Speed devices.

Support

The core as delivered is warranted against defects for 90 days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

Extensive verification has been performed, using code coverage tests, simulation with multiple tools, and implementation and testing in an FPGA demonstration system.

Verification has been performed with many different devices from Micron, Samsung, STM and Toshiba.

Deliverables

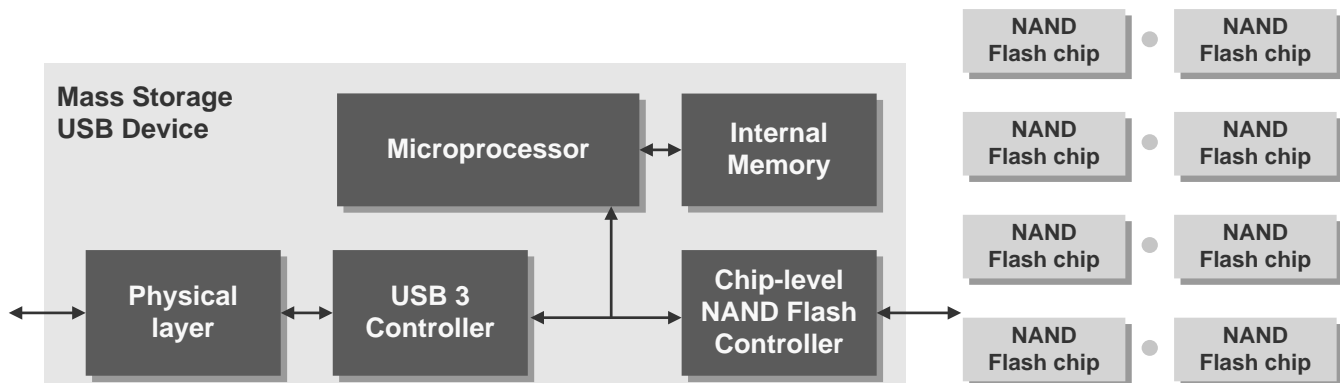
The core includes everything required for successful implementation:

- VHDL or Verilog source code for the core
- An example design that uses the core and illustrates how to build and connect memory and tri-state buffers
- Sophisticated HDL Test Bench that instantiates the example design and related elements
- Interface wrappers when ordered
- Simulation script, vectors, expected results, and comparison utility
- Synthesis scripts
- Comprehensive user documentation, including detailed specifications and a system integration guide

Related Products

NAND Flash Controller Driver – a low-level software driver that represents a first abstraction layer of the core to relieve the higher level application layer from hardware management.

Example Application



For this USB thumb drive, the core is implemented with an internal buffer and tri-state buffers. Data goes through a USB controller, and a microcontroller manages data flow, sets parameters of data transmission for NANDFLASH-CTRL, controls the USB, and handles all aspects connected with a File System implemented in this storage device.