

# CAST

## DDR2-SDRAM-CTRL

### DDR/DDR2 SDRAM Memory Controller Core

The DDR2-SDRAM-CTRL core provides a simplified, pipelined, burst-optimized interface to all industry-standard DDR and DDR-II SDRAM devices currently available, including Mobile SDRAMs. It features:

- **Simplicity.** All required management, initialization, address and burst handling procedures are done by the core. The control, write-data, and read-data paths are split, enabling higher performance and easier integration.
- **Performance.** The core achieves maximum bandwidth utilization through pipelined and parallel architectural design practices.
- **Flexibility.** All memory parameters (timing parameters, memory size parameters, mobile-DDR support, auto-refresh policies, etc.) are runtime configurable.
- **Easier Integration.** Most necessary related components—DDR/DDR-II Controller, data-path FIFOs, DLLs—come built into the core, and some FPGA versions even include a PHY (the ASIC version supports industry-standard PHYs).

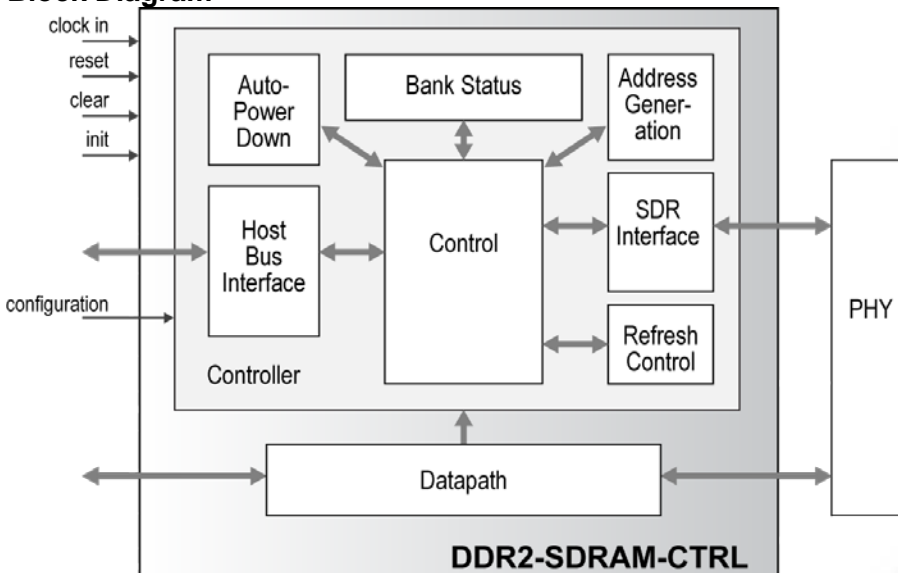
The core has been carefully designed and rigorously verified, and is delivered with comprehensive documentation and a complete verification environment. Representative ASIC results show it to be quite competitive, requiring under 14,500 gates and running at 400 MHz.

### Applications

Any application requiring efficient, high performance access to DDR / DDR-II SDRAM memory, including:

- Processor Interfaces
- Networking
- Video / Image Processing

### Block Diagram



### Features

- Interfaces to all industry standard DDR and DDR-II SDRAM DIMMs and chips, including Mobile SDRAMs.
- High-performance architecture, with a three-stage processing queue for maximum bandwidth utilization.
- Pipelined design facilitates integration and enables high clock rates.
- Includes power-down and self-refresh, critical for low-power applications.
- Datapath logic with small FIFOs, enables handshaking mechanism for enhanced performance and easier integration.
- Two different PHY implementations available: an advanced delayed-DQS capture mechanism with per-bit deskew, and a delayed-clock capture with dual-port synchronizing FIFO.
- Utilizes per-bank status monitoring.
- Incorporates a programmable auto-precharge mechanism.
- Incorporates a programmable automatic refresh policy.
- Supports up to eight chip-selects, up to eight banks per chip, twelve to fifteen row bits, and nine to twelve columns bits.
- Runtime-configurable parameters ensure flexibility: eleven timing parameters, CAS latency, Burst Length, Row bits, Column bits, Bank bits, number of CSs, Extended-Mode-Registers' values, registered-DIMM support, power-saving and auto-precharge mechanism activation.
- Flexible user-interface, with split command, write-data and read-data paths. All paths support hand-shaking mechanisms.
- Multi-burst access support: access requests can have any size burst lengths from 1 to 65536; the core segments these into an appropriate number of SDRAM bursts.
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)

## Functional Description

After power-up the SDRAM device(s) are initialized and then physical-layer calibration commences. After the calibration phase is complete the controller is ready to serve read and write requests.

Requests are served in a pipelined mode, that is, while a request is in progress, another request can be issued. Write and read data are conveyed/received to/from the controller via separate interfaces with distinct handshaking signals.

The DDR2-SDRAM-CTRL core incorporates a parallel auto-close mechanism, which precharges active SDRAM banks that are currently inactive. It also incorporates an Auto-Power-Down & Auto-Self-Refresh mechanism which sets the SDRAM device into "power-down" mode after a configurable time of inactivity. When in power-down mode and if a user or auto-refresh request is received, the SDRAM is set back into normal-mode and the request is served. If an additional time of inactivity is observed, the SDRAM device(s) are set into self-refresh mode, during which the internal SDRAM self-refresh mechanism is used. During this mode, most of the internal circuitry is "frozen", dropping power dissipation to a minimum. And finally, it also takes care of SDRAM refresh requirements.

## Implementation Results

The core has been evaluated in a variety of technologies. The following are representative ASIC results (also see FPGA results on the web site.) They were generated with a 32-bit wide DDR data-bus. Two memories (32x64 and 32x72) are also required for the read and write data-paths respectively. The depth of these memories can be reduced to 16 or less, depending on the required performance and data traffic profile.

ASIC Technology	Approx. Area	NAND2 Size	Gate Size Equiv.	Frequency (MHz)
TSMC 0.09g	40,219	2.8224	14,250	400
TSMC 0.13g	73,054	5.0922	14,346	400
TSMC 0.18g	170,368	9.9792	17,072	400

*Note: The actual cell area and NAND2 divider value used to derive Approximate Area are included since calculation methods for this vary.*

## Support

The core as delivered is warranted against defects for three years from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. It has also been proven in FPGA prototyping boards.

## Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Simulation script, vectors and expected results.
- Vector generation Software
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide