

CAST



IR-RC5-E and -D

Infrared Encoder and Decoder Cores

This pair of cores implements an Encoder and a Decoder for Consumer IR (CIR) infrared remote control signals using the popular RC5 IR protocol, originally developed by Philips. The cores are available individually or together.

The Encoder accepts data and control signals, encodes commands following the RC5 protocol, and outputs the commands to a suitable LED or photodiode transmission circuit. Following the RC5 protocol, the core transmits a five-bit address and a six-bit command. The simple serial input interface eases system integration, and an additional signal allows control of the transmission and indicate when it is complete.

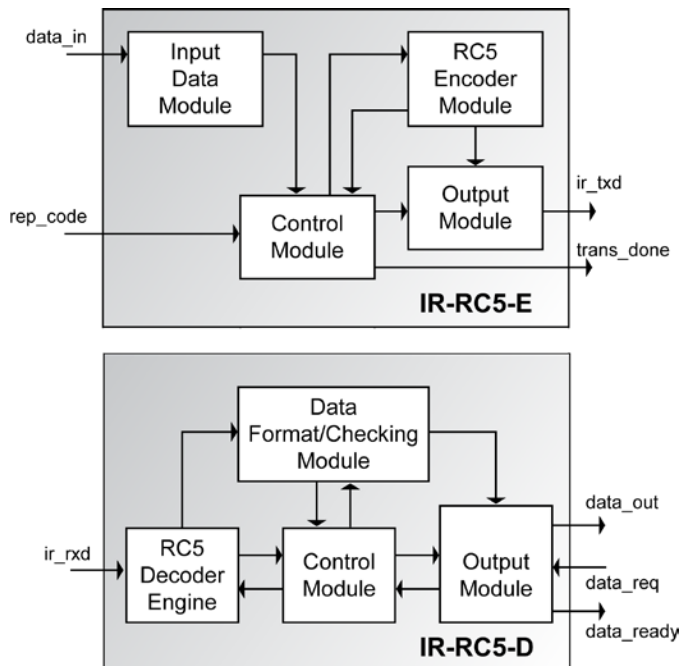
The Decoder receives data from a photodiode or other infrared receiver. The core decodes the IR data and transmits a simple serial output signal. Handshaking signals give the user full control over the transmitted data. An extra output identifies repeating signals for processing efficiency.

The flexible cores are designed for easy system integration, with simple control interfaces. UART and AMBA APB interfaces are also available. The cores are available in HDL source code for ASICs or optimized netlists for FPGAs. Implementation results show them to be area-efficient, requiring for example 55 slices for the Encoder and 99 slices for the Decoder in a Virtex-4 device.

Applications

The cores are suitable for a wide variety of consumer products and other low-speed infrared control applications, including televisions, home theater systems, DVD players and recorders, and video game consoles.

Block Diagram



Features

- 5-bit address and 6-bit command length
- Bi-phase coding (also known as Manchester coding)
- Carrier frequency of 36 kHz as per the RC5 standard
- Fully synchronous design

Encoder Features

- Generic parameter ACTIVE_LEVEL enables consistency with different types of IR transmitters
- Serial input data interface
- UART standard input data interface available; other interfaces available upon request (parallel, APB and others)

Decoder Features

- Internal parameters enable fine tuning for use with different types of IR transmitters:
 - specify the active level,
 - specify the number of clock pulses needed to create the 38 kHz internal signal, and
 - specify the size of the counter used to generate the 38 kHz internal signal
- Complex system of error codes allows easy detection of potential errors and glitches during transmission
- Additional output data interfaces are available now: UART standard, AMBA APB
- Parallel and custom output interfaces available upon request

Functional Description

The cores implement the principles of the RC5 IR protocol, which has been used in hundreds of consumer products for several years.

RC5 IR Encoder

With this protocol, the Encoder transmits a five-bit address and a 6-bit command. Control signals make it easy to manage the transfer of data to the Encoder and then the beginning of its IR transmission. The serial input interface ensures simplicity and easy system integration. An additional output signal indicates when the transmission is completed. As shown in the block diagram, the Encoder core has the following major functional elements.

Input Data Module — provides the serial communication channel for the incoming data.

Control Module — controls the core by sending information about any required repeat signal transmission, end of transmission etc.

RC5 Encoder Engine — converts the incoming stream into the RC5 format.

Output Module — controls the output data stream.

RC5 IR Decoder

The Decoder core receives an 8-bit address and an 8-bit command. The core decodes the data, formats it, and sends it to the user. As shown in the block diagram, the core has the following major functional elements.

RC5 Decoder Engine

Decodes the received data stream, and ensures that only appropriate RC5 protocol pulses are considered. It checks for inappropriate data glitches and reports their absence the user through the error code output signal.

Data Format Module

Collects the decoded data into a 5-bit address and a 6-bit command format.

Control Module

Ensures correct functionality among all the components, sending decoding status from the RC5 Decoder Engine to the other modules, controlling the output interface, etc.

Output Module

Responsible for the serial data transmission of the decoded data stream. Uses a handshaking mechanism to give the user maximum flexibility. An additional output signal gives information about a received repeat signal.

Implementation Results

The RC5 Encoder and Decoder have been evaluated in a variety of technologies. The following are representative Xilinx results optimized for area.

| Encoder | Slices | Performance (MHz) | Memory /Special Features | GCLK | I/O | ISE Version |
|---------------------------|--------|-------------------|--------------------------|------|-----|-------------|
| Spartan-3E XC3S1200E-5 | 80 | 147 | - | 1 | 8 | 12.2i |
| Spartan-6 XC6SLX25-3 | 29 | 236 | - | 1 | 8 | 12.2i |
| Virtex-4 XC4VFX60-12 | 56 | 120 | - | 1 | 8 | 8.2.03i |
| Virtex-5 XC5VLX30-3 | 31 | 355 | - | 1 | 8 | 12.2i |
| Virtex-6 XC6VLX130T-3 | 28 | 413 | - | 1 | 8 | 12.2i |
| Decoder | Slices | Performance (MHz) | Memory /Special Features | GCLK | I/O | ISE Version |
| Spartan-3E XC3S1200E-5 | 141 | 139 | - | 1 | 11 | 12.2i |
| Spartan-6 XC6SLX25-3 | 43 | 214 | - | 1 | 11 | 12.2i |
| Virtex-4 XC4VFX60-12 | 99 | 196 | - | 1 | 11 | 8.2.03i |
| Virtex-5 XC5VLX30-3 | 39 | 325 | - | 1 | 11 | 12.2i |
| Virtex-6 XC6VLX130T-3 | 40 | 428 | - | 1 | 11 | 12.2i |

Support

The cores as delivered are warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The cores have been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The cores are available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Sophisticated HDL Testbench
- Simulation script, vectors and expected results.
- Vector generation Software
- Place and route script
- Comprehensive user documentation