

CAST



IR-NEC-E and -D

Infrared Encoder and Decoder Cores

This pair of cores implements an Encoder and a Decoder for Consumer IR (CIR) infrared remote control signals using the popular NEC IR protocol. The cores are available individually or together.

The Encoder accepts data and control signals, encodes commands following the NEC protocol, and outputs the commands to a suitable LED or photodiode transmission circuit. The simple serial input interface eases system integration, and an additional control signal can easily send a repeat signal. A supplementary output signal is available to provide additional transmission information. Following the NEC protocol, the core transmits each address and command twice to increase reliability.

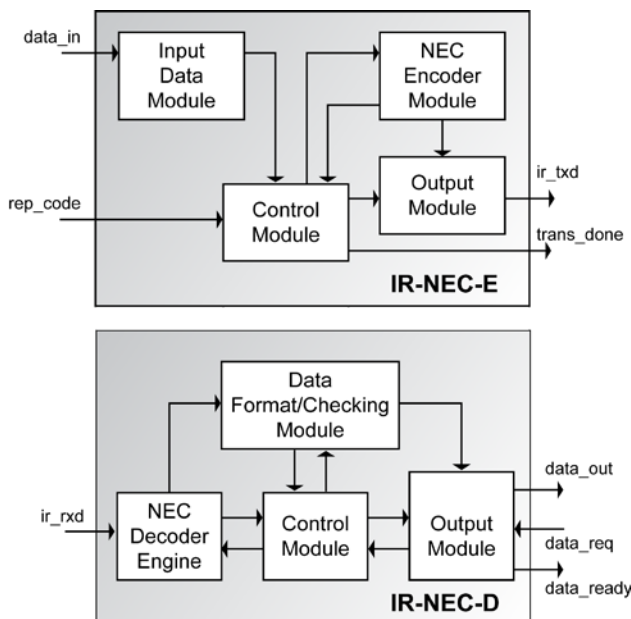
The Decoder receives data from a photodiode or other infrared receiver. It compares the incoming IR data stream with the inverted form of that data for greater reliability. A complex system of error detection and an error reporting signal help the user quickly identify the source of any errors. The decoded data is transmitted through a simple serial output signal, and handshaking signals give the user full control over the transmitted data. An extra output identifies repeating signals for processing efficiency.

The flexible cores are designed for easy system integration, with simple control interfaces. UART and AMBA APB interfaces are also available. The cores are available in HDL source code for ASICs or optimized netlists for FPGAs. Implementation results show them to be area-efficient, requiring for example 123 slices for the Encoder and 146 slices for the Decoder in a Virtex-4 device.

Applications

The cores are suitable for a wide variety of consumer products and other low-speed infrared control applications, including televisions, home theater systems, DVD players and recorders, and video game consoles.

Block Diagram



Features

- 8-bit address and 8-bit command length
- Carrier frequency of 38 kHz as per the NEC standard
- Pulse distance modulation
- Fully synchronous design

Encoder Features

- Address and command are transmitted twice for reliability
- Generic parameter ACTIVE_LEVEL enables consistency with different types of IR transmitters
- Serial input data interface
- UART standard input data interface available; interfaces available upon request (parallel, APB and others)

Decoder Features

- Received address and command are compared with received inverted address and command to increase transmission reliability
- Internal clock generator provides flexibility with the clock signal value (which still must be a multiple of 38 MHz)
- Internal parameters enable fine tuning for use with different types of IR transmitters:
 - specify the active level,
 - specify the number of clock pulses needed to create the 38 kHz internal signal, and
 - specify the size of the counter used to generate the 38 kHz internal signal
- Complex system of error codes allows easy detection of potential errors and glitches during transmission
- Serial output data interface
- Additional output data interfaces are available now: UART standard, AMBA APB
- Parallel and custom output interfaces available upon request

Functional Description

The cores implement the principles of the NEC IR protocol, which has been used in hundreds of consumer products for several years.

NEC IR Encoder

With this protocol, the Encoder transmits an address and command twice to increase reliability. Control signals make it easy to manage the transfer of data to the Encoder and then the beginning of its IR transmission. The serial input interface ensures simplicity and easy system integration. An additional control signal makes it easy to send a repeat code, and a supplementary output signal can provide additional transmission information to the user. As shown in the block diagram, the Encoder core has the following major functional elements.

Input Data Module — provides the serial communication channel for the incoming data.

Control Module — controls the core by sending information about any required repeat signal transmission, end of transmission etc.

NEC Encoder Engine — converts the incoming stream into the NEC format.

Output Module — controls the output data stream.

NEC IR Decoder

The Decoder core receives an 8-bit address and an 8-bit command. The core decodes the data, formats it, and sends it to the user. As shown in the block diagram, the core has the following major functional elements.

NEC Decoder Engine — decodes the received data stream and ensures that only appropriate NEC protocol pulses are considered. Catches all glitches and any data in an unsupported format and notifies the user through the error code output signal.

Data Format/Checking Module — compares the decoded data stream with its inverted version, and indicates any errors through the error code output.

Control Module — ensures correct functionality among all the components, sending decoding status from the NEC Decoder Engine to the other modules, controlling the output interface, etc.

Output Module — responsible for the serial data transmission of the decoded data stream. Uses a handshaking mechanism to give the user maximum flexibility. An additional output signal gives information about a received repeat signal.

Implementation Results

The IR-NEC Encoder and Decoder have been evaluated in a variety of technologies. The following are representative Xilinx results with Slices optimized for area.

Encoder	Slices	Performance (MHz)	Memory /Special Features	GCLK	I/O	ISE Version
Spartan-3E XC3S1200E-5	140	147	-	1	8	12.2i
Spartan-6 XC6SLX25-3	38	178	-	1	8	12.2i
Virtex-4 XC4VFX60-12	123	170	-	1	8	8.2.03i
Virtex-5 XC5VLX30-3	46	330	-	1	8	12.2i
Virtex-6 XC6VLX130T-3	34	388	-	1	8	12.2i
Decoder	Slices	Performance (MHz)	Memory /Special Features	GCLK	I/O	ISE Version
Spartan-3E XC3S1200E-5	180	131	-	1	11	12.2i
Spartan-6 XC6SLX25-3	65	197	-	1	11	12.2i
Virtex-4 XC4VFX60-12	146	150	-	1	11	8.2.03i
Virtex-5 XC5VLX30-3	75	280	-	1	11	12.2i
Virtex-6 XC6VLX130T-3	54	373	-	1	11	12.2i

Support

The cores as delivered are warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The cores have been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The cores are available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Sophisticated HDL Testbench
- Simulation script, vectors and expected results.
- Vector generation Software
- Place and route script
- Comprehensive user documentation