

CAST



USBSS-DEV

USB 3.0 SuperSpeed Device Controller IP Core

This IP core implements a device controller that conforms to the USB 3.0 SuperSpeed specification.

The SuperSpeed 3.0 USB enables data transfers up to 5 Gbps, while also reducing power requirements. Its use of Sync-N-Go technology reduces user wait-time, and it is backwards-compatible with USB 2.0. The core handles byte transfer autonomously, and bridges the USB interface to an OCP interface for straightforward system integration (AMBA® AHB and other system interfaces are also available). The USBSS-DEV can be readily customized and optimized for a wide range of specific system applications.

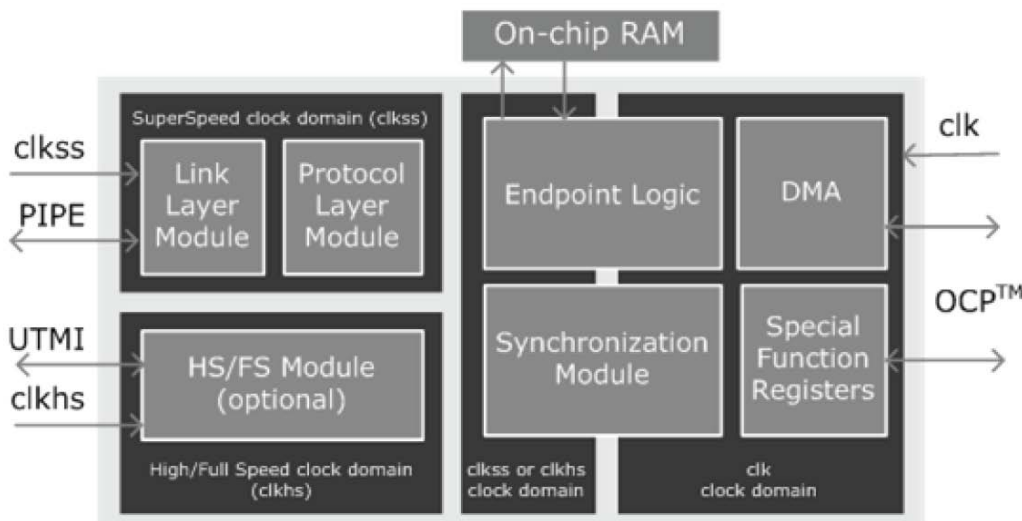
The core is developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with positive-edge clocking, a synchronous reset and no internal tri-states; therefore, scan insertion is straightforward.

Applications

The SuperSpeed USB 3.0 device controller core is suitable for a variety of applications, including:

- mass storage products
- audio/video systems
- communication devices
- digital cameras
- networking
- digital media controllers

Block Diagram



Features

- USB 3.0 Specification Rev. 1.0 compliant
- 32-bit OCP Slave interface implemented as a basic microprocessor interface
- Integrated DMA controller with a 32-bit OCP Master Interface
- USB 3.0 PIPE interface to PHY (32-bit)
- Control transfers supported by Endpoint 0
- Up to 15 IN and 15 OUT configurable/ programmable endpoints
- Synchronous Single Port RAM interface for endpoint buffers
- Full Power Management capabilities (U1, U2 & U3) with LFPS support
- Bulk Stream support
- Backwards compatibility achieved through integration with the CAST USB 2.0 (Hi and Full-Speed) Device controller

Benefits

- Complete hardware and software solution
- High level of configurability
- Industry standard interfaces that simplify system integration
- Verilog coding style for true technology independence
- Customization to fit user needs
- Flexible licensing schemes

Certification



- This core has achieved USB-IF Certification

Functional Description

The USBSS-DEV core is partitioned into modules, as shown in the block diagram and described below:

Link Layer Module

This module works in the USB clock domain. The link layer's responsibility is to maintain the link connectivity to ensure reliable header packet exchange, as required by the USB 3.0 specification.

The link layer module builds and transmits packets. It has a header buffer included to store the header packets during the link management process.

This module also performs entry & exit sequences for low power states and initiates/detects inband reset.

Protocol Layer Module

The Protocol layer manages communication between the host and the protocol layer. This module services SET ADDRESS request, while other requests are serviced by the software. It works in the USB clock domain.

Hi-Speed and Full-Speed Module (optional)

This component contains all necessary logic required to handle USB 2.0 transactions. It can be connected directly with the external USB2.0 transceiver that is compatible with the UTMI Specification.

Endpoint Logic

Endpoint logic generates read/write signals for one single port synchronous RAM, which is used as an on-chip internal buffer for both IN and OUT endpoints. This module contains all endpoint registers and is responsible for the management of the internal buffers.

Synchronization Module

Cross clock domain synchronization module.

DMA

Integrated DMA controller. The DMA is used to control a data transfer between endpoint buffers (on-chip RAM) and external memory.

Special Function Registers

SFRs module contains a set of Special Function Registers which are used to control the USBSS-DEV operation.

Support

The core, as delivered, is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, beginning with the first interaction. Additional maintenance and support options are available.

Implementation Results

USBSS-DEV reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results with one bidirectional control endpoint, two other endpoints, and 64kB on-chip buffer memory.

Xilinx Device	Slices	BRAM	Special Features	I/Os	pclk/cik (MHz)	ISE
Virtex-5 5VFX70T-3	4796	8	3 DSP48	317	125/79	12.2i
Virtex-6 6VLX75T-3	4821	8	3 DSP48	317	125/62	12.2i

Verification

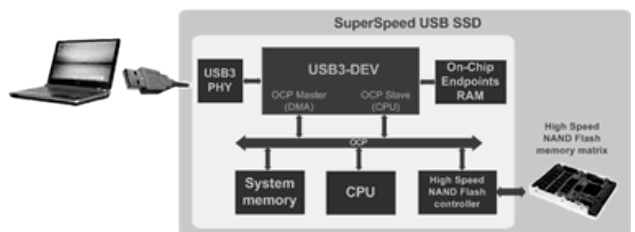
The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Extensive SystemC Test Bench that includes: a complete sample design, external endpoint buffer, and a USB3.0 device TLM model
- Sophisticated HDL Testbench including external FIFOs, buffers, models of interfaces, and the core
- Simulation script, vectors, and expected results
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide

Example Application



Here the USBSS-DEV is implemented with an internal single-port RAM. The core works as a USB peripheral device, transmitting data between the fast flash memory and PC using the SuperSpeed USB connection. USB data packets are transferred between the on-chip endpoint memory and system memory using an integrated USB protocol-aware DMA controller. The CPU controls the settings of endpoints and service interrupts.