

CAST



USBHS-OTG-SD

USB2.0 On-The-Go Controller Core

Implements a hi-speed USB OTG port that can serve as a host (for a single device) or as a peripheral when connected to other USB devices.

This dual-role behavior conforms to the USB 2.0 specification and its On-The-Go Supplement. The core is designed for processing efficiency — with hardware implementing the Host Negotiation Protocol, Session Request Protocol, and other critical functions — and is competitive in performance and area usage.

Standard USB transceivers can be used through the core's UTMI+ Level 2 interface, and a UTMI+ Low Pin Interface (ULPI) is available. The core's system connection is through a standard PVIC interface (AMBA™ and other standard interfaces are also available). Configurable endpoints and other USB characteristics can be customized prior to synthesis to match the core to a specific application. The core also supports USB power saving functions.

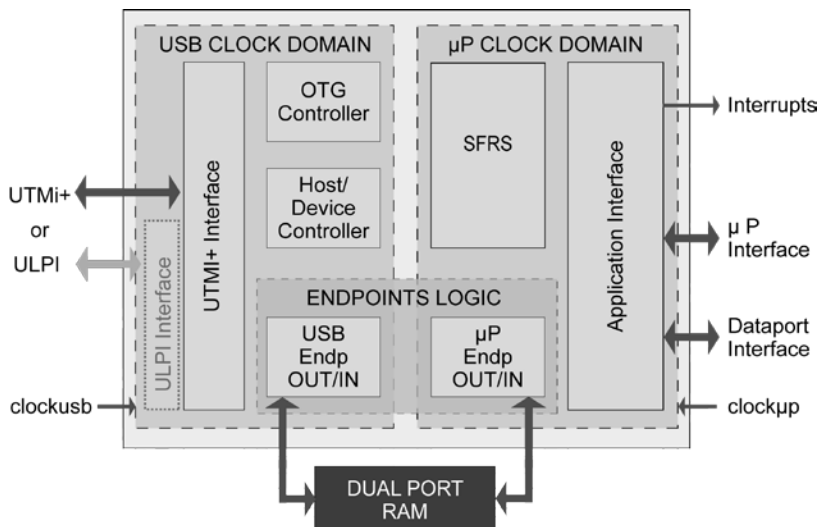
The USBHS-OTG-SD is a testable, microcode-free design developed for reuse in ASICs and FPGAs. A complete test environment helps designers verify the functioning and compliance of the core, and includes a USB PHY behavioral model to facilitate transaction simulation.

Applications

USB OTG is primarily intended for portable devices that may function as a host or a peripheral depending on how they are connected. The dual-role device uses a USB mini-AB port that can receive a mini-A plug to trigger host mode or a mini-B plug for peripheral mode. For example:

- A PDA connects to a PC for contacts and calendar syncing (peripheral mode), to a printer (host mode), or to another PDA with USB OTG (host and device negotiated as needed).
- Two MP3 players with OTG ports might connect directly, one acting as a host to copy files from the other acting as a peripheral.

Block Diagram



Features

- Complies with the USB 2.0 specification and its On-The-Go supplement
- Supports one Low-Speed, Full-Speed, or High-Speed peripheral device in Host mode
- Supports Full-Speed and High-Speed data transfer in Peripheral mode
- Provides hardware-based support for the Host Negotiation Protocol (HNP) and the Session Request Protocol (SRP)
- Includes endpoint 0 for USB control transfers
- Configurable for up to 15 IN and 15 OUT additional endpoints, each with:
 - Configurable and programmable size & buffering (single, double, triple or quad)
 - Programmable type (bulk, ISO, interrupt)
- UTMI+ Level 2 (USB 2.0 Transceiver Macrocell Interface Plus) for use with any compliant transceiver macrocell
- Optional ULPI (UTMI+ Low Pin Interface)
- 32-bit Peripheral Virtual Component Interface (PVCI) to microprocessor (other standard interfaces available)



The single-port RAM version of this core has received USB-IF certification (through development partner Evatronix).

- Offers direct access to the endpoint buffers via a configurable 16/32-bit dataport interface
- Optional software stack
- Ready for an external DMA module
- Synchronous dual-port RAM interface for endpoint buffers (single-port RAM version available)
- Suspend and resume power management functions
- Remote wake-up function
- Strictly synchronous design with positive-edge clocking, no internal tri-states and a synchronous reset; therefore scan insertion is straightforward.
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)

Functional Description

The USBHS-OTG-SD core is partitioned into modules as shown in the block diagram and described below.

UTMI+ Interface

The core requires an external transceiver that is compatible with the USB 2.0 UTMI+ specification (Philips USB 2.0 Transceiver Macrocell Interface Plus, version 1.0).

OTG Controller

Supports the tasks specified in the OTG Supplement. It includes hardware implementations of the Host Negotiation Protocol (HNP) and the Session Request Protocol (SRP), and special function registers for their control.

This block manages the upstream and downstream activity on the USB OTG port, and chooses between them. The default operation mode is determined by which end of the USB OTG cable the user has inserted into the port: one end makes the core operate as a host, the other end a peripheral.

Host Controller

Functions when the core operates as a host, with the main tasks of generating suspend/resume and USB reset signals, generating Start of Frame (SOF) tokens, managing USB data transactions, and generating host interrupts. It includes a hardware Host Transaction Scheduler and a frame generator.

Device (Peripheral Mode) Controller

Supports all types of USB 2.0 data transfers in peripheral mode, and performs additional standard operations such as receiving SOF tokens, detecting suspend/resume signals, and controlling the remote wakeup function.

Endpoints Logic Blocks

Includes endpoint 0 to support USB control requests, and up to 15 additional endpoints for custom requests. Supports all four types of USB data transfers:

- Control transfer – interactions with standard endpoint 0,
- Interrupt transfer – transfer for small, non-periodic, low-frequency data,
- Bulk transfer – transfer for a large amount of data, and
- Isochronous transfer – for applications requiring constant data transfer rates.

Generates read/write signals for two dual synchronous RAM blocks, one for OUT and one for IN endpoints. The number, size, and buffering of up to 15 IN and 15 OUT endpoints can be configured before synthesis.

SFRS

Contains a set of Special Function Registers that control the core's operation.

Application Interface

Provides an interface to the system microprocessor using PPCI, the VSIA's Peripheral Virtual Component Interface standard (OCP, AMBA, and other standard interfaces are available). Also generates interrupt signals for the microprocessor, and includes the Dataport Interface that provides direct access to the endpoint buffers.

Software

A complete software stack with the most popular device classes is available. It has been designed for portability in a variety of embedded applications.

Implementation Results

USBHS_OTG_SD reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results optimized for speed and configured for operation with IN 1 - 512 bytes dual buffered and OUT 1 - 512 bytes dual buffered. uP data width: 32-bit; USB data width: 16-bit.

Xilinx Device	Slices	BRAM	IOB	Fmax clk usb	Fmax clk up	ISE
Spartan-3E 3S1600E-5	2951	8	222	30 MHz	61 MHz	12.2i
Spartan-6 6SLX100-3	1249	8	223	30 MHz	100 MHz	12.2i
Virtex-5 5V5X95T-2	1676	8	222	30 MHz	147 MHz	12.2i
Virtex-6 6VLX130T-3	1308	8	222	30 MHz	201 MHz	12.2i

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements, and has been implemented and tested in a demonstration application.

Deliverables

The core includes everything required for successful implementation: The Xilinx Implementation includes:

- Post-synthesis EDIF netlist
- An example chip implementation
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001) including external endpoint buffers, a USB PHY behavioral model, and a clock generator
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide