

CAST

USBHS-OTG-MPD

USB Hi-Speed On-The-Go Controller for Multiple Peripheral Devices Core

Features

- Complies with the USB 2.0 specification and On-The-Go supplement to the USB 2.0 specification
- In Host Mode, supports Hi-Speed hubs and multiple Low-Speed, Full-Speed or Hi-Speed peripheral devices
- In Device Mode, supports Full-Speed and Hi-Speed data transfer
- Supports USB split transactions
- Support for Host Negotiation Protocol and Session Request Protocol (in hardware)
- Control transfers supported by Endpoint 0
- UTMI+ (Level3) or ULPI Transceiver Macrocell Interface
- 32-bit AMBA™ AHB slave interface
- Integrated multichannel DMA module
 - 32-bit AMBA™ AHB master interface
 - USB protocol-aware DMA engine
- Synchronous RAM interface for endpoint FIFOs
- Suspend and resume power managements functions
- Remote Wake-Up function

Configurability

- Configurable for up to 15 IN and 15 OUT endpoints
 - Configurable/programmable number of endpoints
 - Programmable type of endpoints (bulk, ISO, interrupt)
- Programmable TX FIFO size and RX FIFO size
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)

Certification support service

To confirm full compliance of our USB controller cores to the USB specification we successfully submitted many reference designs containing our cores to the USB Implementer Forum certification procedures. Experience gained in this process allows us to assist our licensees in achieving USB compliance.



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The USBHS-OTG-MPD core implements a hi-speed USB port that can serve as either a host or a peripheral when connected to other USB devices. It features an integrated direct memory access (DMA) controller for efficient, autonomous data transfer, and can support USB hubs and multiple peripheral devices in host mode.

The core's dual-role behavior conforms to the On-The-Go Supplement to the USB 2.0 specification. The core is designed for processing efficiency, with hardware state machines implementing the Host Negotiation Protocol, Session Request Protocol, and other critical functions, and is competitive in both performance and area usage.

Standard USB transceivers can be used through the core's UTMI+ interface. The core's system connection is an AMBA™ AHB slave interface (other standard interfaces are also available). The number and qualities of up to 15 configurable endpoints and other USB characteristics can be customized prior to synthesis to match the core to a specific application, and the core supports USB power saving functions.

The USBHS-OTG-MPD is a testable, microcode-free design developed for reuse in ASICs and FPGAs. A complete test environment helps designers verify the functioning and compliance of the core, and includes a behavioral model of the PHY software layer to allow easy transaction simulation.

Applications

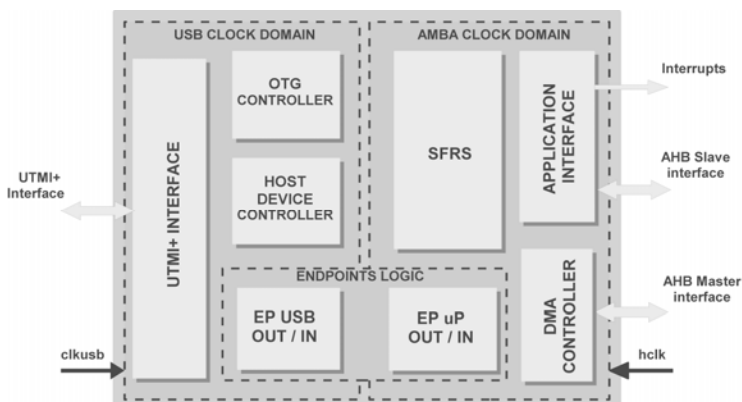
Enables the direct connection of digital products without a computer host, for example:

- Connecting a digital camera directly to a printer for prints or to a cellular phone for Internet photo sharing.
- Connecting a digital music player to a CD player to download songs, to a set of speakers to play them, and to a disk burner to archive custom playlists.

Software

Two complete software stacks supporting both host and device functions along with several of the most popular device classes are available. One stack supports hubs as well as all other functions. The second is a simpler version with no hub support. Both have been designed for portability in a variety of embedded applications.

Block Diagram



Functional Description

The core is partitioned into modules as shown on the block diagram and described below.

OTG Controller

The dual-role core can act as a USB host or a USB peripheral device. It supports all tasks specified in the OTG supplement and implements the downstream and upstream ports. It provides the hardware implementation of the HNP (Host Negotiation Protocol) and SRP (Session Request Protocol). The SFRS block controls the HNP and SRP.

UTMI+ / ULPI Interfaces

The core requires an external transceiver that is compatible with the USB 2.0 UTMI+ specification (Philips USB 2.0 Transceiver Macrocell Interface Plus, version 1.0). A ULPI interface is available upon request.

Endpoints Logic

Coordinates use of the same endpoint resources in host and peripheral modes. It is fully configurable: the number of endpoints, and the size of the transmit and receive FIFOs can be adjusted to achieve a specific implementation.

Host Controller

Functions when the core works as a USB host. Its main tasks are:

- Generation of suspend/resume signaling and USB reset
- Generation of SOF tokens
- USB data transactions
- Generation of host interrupts

It also contains the Host Transaction Scheduler (HTS), which analyzes how many endpoints wait for service and decides which endpoints will be serviced in the current (m)frame and which in the next (m)frame.

Device Controller

Implements the tasks of a USB device:

- USB data transactions
- Suspend/resume behavior
- Generation of interrupts

DMA Controller

Controls data transfer between the endpoint buffers and system memory.

- 32-bit AMBA™ AHB master interface
- Multichannel DMA
- Interrupt request after USB transfer (multiple USB transactions) is completed

Application Interface

This block contains the interrupt controller, which generates interrupt signals for the microprocessor and the 32-bit AMBA™ AHB slave interface.

Implementation Results

The core has been evaluated in a variety of technologies and devices. Synthesis results targeting an indicative 0.18u ASIC process and implementing four endpoints show that the core requires just 45K gates and runs at 200 MHz.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

PHY/transceiver operability program

The USB controllers have been used with a number of third party PHYs and transceiver ICs. CAST partner Evatronix performs USB-IF compliance pre-testing to discover and resolve any issues regarding interoperability between the controllers and third party USB PHYs.

Verification

The core has been verified through extensive simulation using a large set of test vectors and reference results, and through rigorous code coverage measurements.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code.
- An example chip implementation, which uses the core in a sample system
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001) including external endpoint buffers, a bus/behavioral model USB stimulator (PHY), and a clock generator
- Simulation scripts, vectors, and expected results.
- Synthesis script.
- Comprehensive user documentation, including detailed specifications and a system integration guide.