

# CAST

## USBHS-HUB

### USB Hi-Speed Embedded Hub Controller Core

The USBHS-HUB core implements a hi-speed configurable USB Hub controller that can serve as an interface between a USB host and multiple USB peripheral devices, each operating at different signaling frequencies: Low-, Full-, or High-Speed.

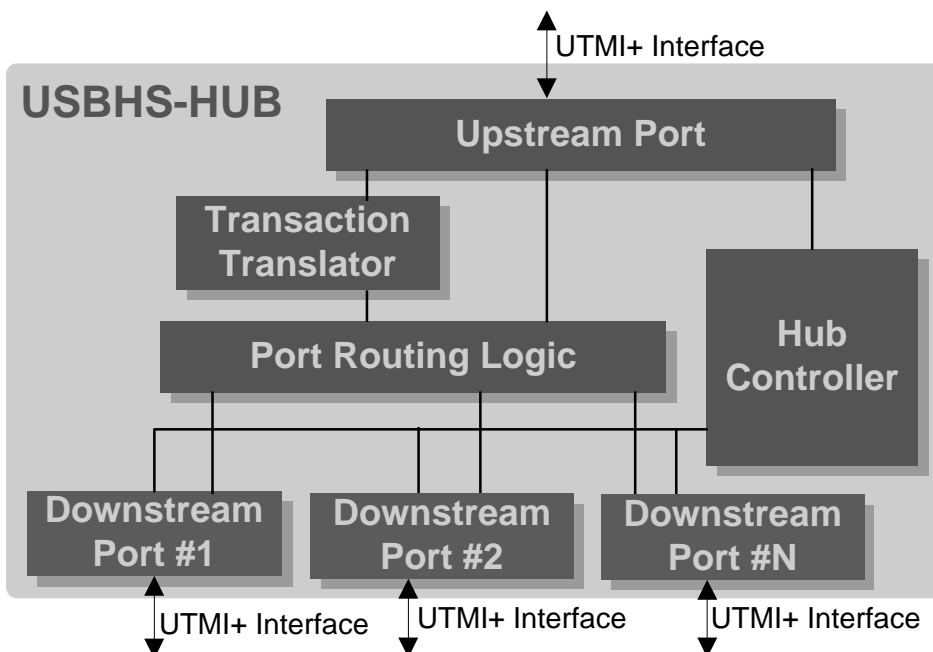
The main functional features of the core include connectivity behavior, connect/disconnect detection, power management, bus fault detection and recovery, as well as support for USB transactions. The core contains the Transaction Translator module that translates Hi-Speed upstream port transactions to Low-/Full-Speed downstream ports transactions.

The USBHS-HUB is a testable, microcode-free design developed for reuse in ASICs and FPGAs. A complete test environment helps designers verify the functioning and compliance of the core. Its wide range of configurable features allows customization and optimization for a specific design. The controller is strictly synchronous with positive-edge clocking, a synchronous reset, and no internal tri-states.

#### Applications

- Personal computers
- Docking stations
- Set top boxes
- Personal Digital Assistants (PDAs)
- Mobile phones.

#### Block Diagram



#### Features

- Complies with the USB 2.0 specification
- Supports Hi-Speed, Full-Speed or Low-Speed peripheral devices
- Supports standard and hub-specific requests
- Supports up to 127 downstream ports
- Integrated Transaction Translator for USB Low-/Full-Speed transfers
- Connect/disconnect detection of downstream ports
- Suspend/resume power management functions
- Supports 8-/16-bit UTMI+ Transceiver Macrocell Interface
- Optional 8-bit ULPI Transceiver Macrocell Interface on downstream port

#### Benefits

- Broadens the host controller functionality by allowing connection of Full- and Low-Speed devices without separate OHCI or UHCI host controllers
- Ability for direct on-chip connection to the host without using an external transceiver
- User configurable features
- Wide range of applications

#### Configurability

- Configurable size of the On-Chip Transfer Descriptor memory
- Number of downstream ports
- Number of transaction translator buffers

## Functional Description

The core is partitioned into modules as shown on the block diagram and described below.

### Hub Controller

Contains endpoint0 (EP0) that is used to handle all hub-specific control transfers and endpoint1 (EP1), and the Status Change endpoint which is used to provide status change notifications to the host system. All standard and hub-class specific commands are processed by the configuration/ enumeration Finite State Machine (FSM) that is based on the contents of the ROM memory with the HUB descriptors.

### Transaction Translator

Handles USB 2.0 Split Transactions by providing support for Low-/Full-Speed devices connected to the USBHS-HUB downstream ports. It supports all types of USB transfers (bulk, interrupt, control and isochronous).

### Upstream Port

Handles detection/generation of the USB reset and USB suspend/resume signals. Upstream port logic provides two interfaces - an UTMI interface, which can be connected to an external transceiver, and an UTMI+ interface, which can communicate directly with the USB host controller.

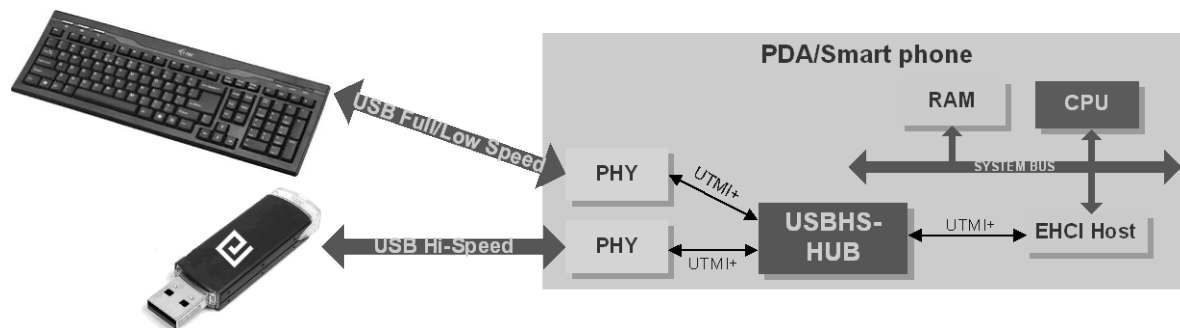
### Port Routing Logic

Used to route Low-/Hi-Speed packets between downstream ports and the upstream port, as well as distribute Low-/Full-Speed packets between downstream ports and Transaction Translator.

### Downstream Port

Contains downstream FSM logic, which is responsible for device connection and speed detection, suspend/resume signaling, and USB reset signaling.

## Application Example



The USBHS-HUB IP core is integrated with a USB Hi-Speed host via an UTMI+ interface to allow connection of Full-/Low-Speed peripheral devices without the OHCI or UHCI companion host controller.

## Implementation Results

The core has been evaluated in a variety of technologies and devices. Synthesis results targeting a TSMC 90nm process and implementing two downstream ports optimized for area show that the core requires just 38K gates (PHY Speed = 30 MHz).

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The core has been verified through extensive simulation using a large set of test vectors and reference results, and through rigorous code coverage measurements.

## Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code.
- An example chip implementation, which uses the core in a sample system
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001) including external endpoint buffers, a bus/behavioral model USB stimulator (PHY), and a clock generator.
- Simulation scripts, vectors, and expected results.
- Synthesis script.
- Comprehensive user documentation, including detailed specifications, a system integration guide and a verification specification.