

CAST

USBHS-DEV

High Speed USB Device Controller Core

The USBHS-DEV core implements a complete high/full-speed (480/12 Mbps) peripheral controller that interfaces to a UTMI USB port transceiver on one side and to a system's microprocessor on the other. It is user-configurable for up to 15 IN and OUT endpoints, and includes power management and remote wake-up functions.

Options include a protocol aware DMA controller, support for a variety of widely used bus interfaces, and a UTMI Low Pin Interface (ULPI).

Designed for easy reuse in ASIC and FPGA implementations, the microcode-free design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset; therefore scan insertion is straightforward.

Applications

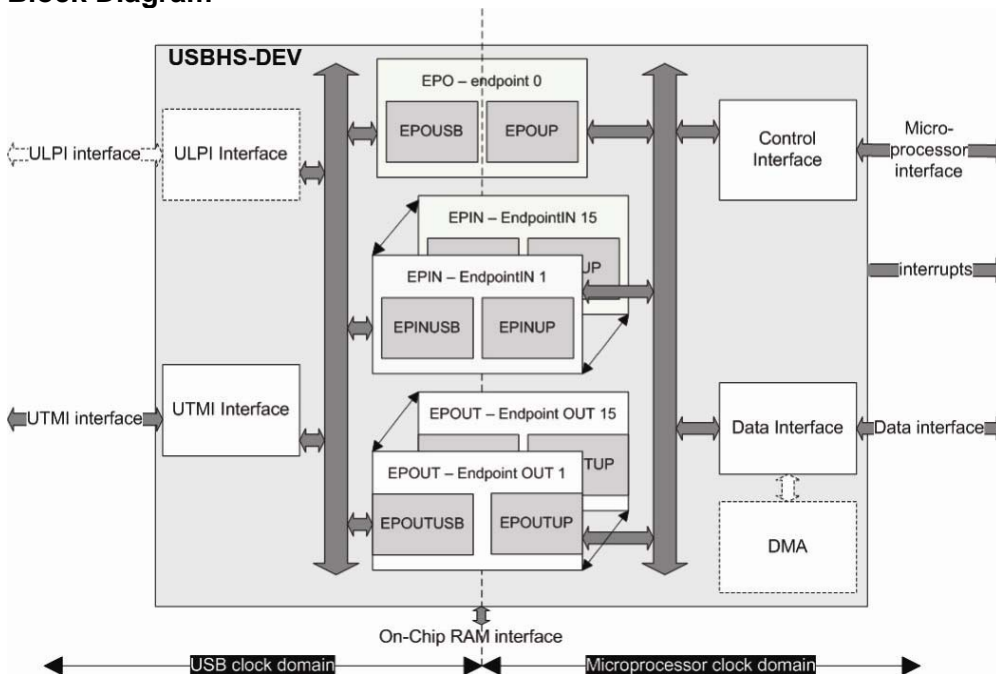
The USBHS-DEV can be utilized in a variety of serial interface applications including:

- Embedded microcontroller systems
- Communication & networking systems
- Digital Media controllers

Software

A complete software stack configurable for the most popular device class is available. It has been designed for portability in a variety of embedded applications. It includes an intuitive Application Programming Interface (API) for application development.

Block Diagram



Features

- Full compliance with the USB 2.0 specification
- Control endpoint 0 — fixed 64 Bytes size
- Configurable for up to 15 IN and 15 OUT endpoints
 - Configurable/programmable number and size of endpoints
 - Configurable/programmable single, double, triple or quad buffering
 - Programmable type of endpoints
- UTMI Transceiver Macrocell Interface; Optional UTMI Low Pin Interface (ULPI)
- Choice of different microprocessor interfaces:
 - AMBA® AHB
 - PPCI
 - Generic
- Configurable 8-, 16-, or 32-bit microprocessor interface
 - Easy integration with a wide range microprocessors and bus architectures
 - Interrupt request signals for application microprocessor
 - Interrupt vector for autovectorized interrupts
- Direct access to the endpoint buffers via configurable 8-, 16-, or 32-bit Slave FIFO interface Ready for external DMA module
- Synchronous RAM interface for FIFOs
- Optional protocol-aware DMA controller with configurable number of channels
- Suspend and resume power management functions
- Remote Wake-Up function
- Optional software stack
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)



Customer products using this core have received USB-IF certification.

Customization

Options available upon request before delivery:

- Microprocessor Interface
- ULPI transceiver interface
- Protocol-aware DMA controller

Implementation Results

Reference designs have been evaluated in a variety of technologies. The following are sample results optimized for area (uP clock = 66 MHz) using a typical configuration of the USBHS-DEV core for a 16-bit USB 2.0 transceiver data bus (UTMI clock = 30 MHz), 32-bit CPU and Slave FIFO buses. This typical configuration includes endpoint 0 and two additional double buffered, 1024-byte endpoints, IN and OUT, as might be used for a USB mass storage device.

ASIC Technology	Approximate Area*
TSMC 0.13 μ m	16,800 gates
TSMC 90 nm	16,550 gates

* 4224 bytes of memory required not included

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001) including external FIFOs, buffers, models of interfaces, vectors for testing the core, and the core
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide