

CAST



USBHS-DEV

High Speed USB Device Controller Core

The USBHS-DEV core implements a complete high/full-speed (480/12 Mbps) peripheral controller that interfaces to a UTMI USB port transceiver on one side and to a system's microprocessor on the other. It is user-configurable for up to 15 IN and OUT endpoints, and includes power management and remote wake-up functions.

Options include a protocol aware DMA controller, support for a variety of widely used bus interfaces, and a UTMI Low Pin Interface (ULPI).

Designed for easy reuse in ASIC and FPGA implementations, the microcode-free design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset.

Applications

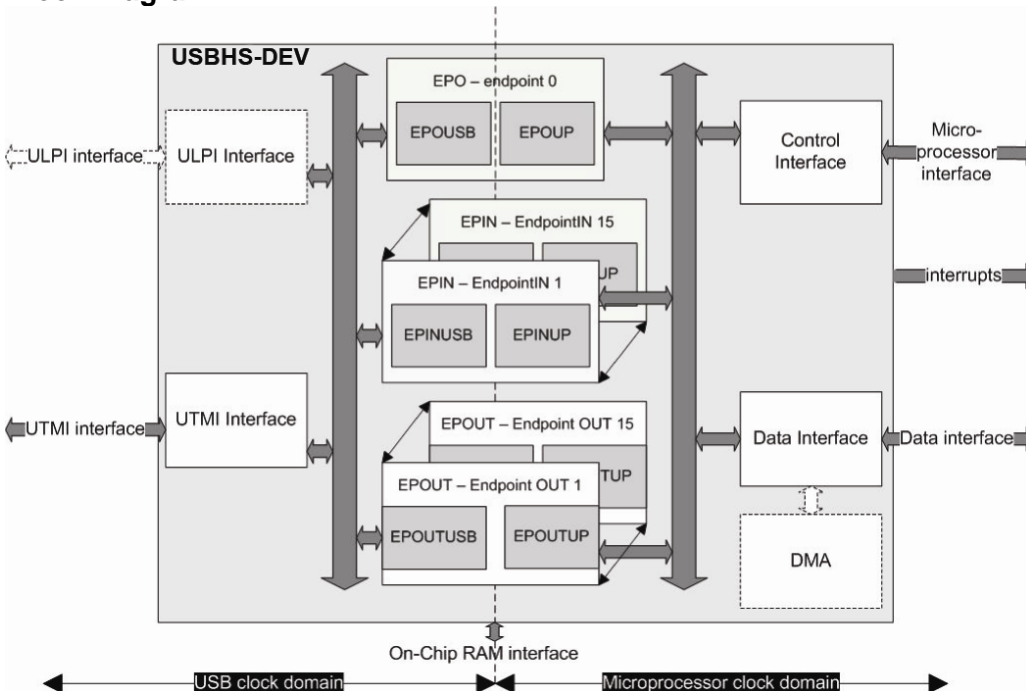
The USBHS-DEV can be utilized in a variety of serial interface applications including:

- Embedded microcontroller systems
- Communication & networking systems
- Digital Media controllers

Software

A complete software stack configurable for the most popular device class is available. It has been designed for portability in a variety of embedded applications. It includes an intuitive Application Programming Interface (API) for application development.

Block Diagram



Features

- Full compliance with the USB 2.0 specification
- Control endpoint 0 — fixed 64 Bytes size
- Configurable for up to 15 IN and 15 OUT endpoints
 - Configurable/programmable number and size of endpoints
 - Configurable/programmable single, double, triple or quad buffering
 - Programmable type of endpoints
- UTMI Transceiver Macrocell Interface; Optional UTMI Low Pin Interface (ULPI)
- Choice of different microprocessor interfaces:
 - AMBA® AHB
 - PPCI
 - Generic
- Configurable 8-, 16-, or 32-bit microprocessor interface
 - Easy integration with a wide range microprocessors and bus architectures
 - Interrupt request signals for application microprocessor
 - Interrupt vector for autovectorized interrupts
- Direct access to the endpoint buffers via configurable 8-, 16-, or 32-bit Slave FIFO interface Ready for external DMA module
- Synchronous RAM interface for FIFOs
- Optional protocol-aware DMA controller with configurable number of channels
- Suspend and resume power management functions
- Remote Wake-Up function
- Optional software stack
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)



Customer products using this core have received USB-IF certification

Customization

Options available upon request before delivery:

- Microprocessor Interface
- ULPI transceiver interface
- Protocol-aware DMA controller

Implementation Results

USBHS-DEV reference designs have been evaluated in a variety of technologies. The following sample Xilinx results were optimized for area and use a minimum configuration for a 16-bit USB 2.0 transceiver data bus (ULPI clock = 30 MHz), a 32-bit processor interface and a 32-bit slave FIFO data bus. This typical minimum configuration includes endpoint 0, 1 IN 1024 bytes and 1 OUT 512 bytes BULK double buffered endpoints, as might be used for a USB mass storage device.

Xilinx Device	Slices	BRAM	IOBs ¹	Fmax uP clock	ISE
Spartan-3E 3S1600E-5	1837	8	258	65 MHz	12.2i
Spartan-6 6SLX100-3	777	8	258	105 MHz	12.2i
Virtex-5 5VFX100T-3	952	4	258	167 MHz	12.2i
Virtex-6 6VLX75T-3	721	8	258	200 MHz	12.2i

¹ Assuming all I/Os are routed off chip

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001) including external FIFOs, buffers, models of interfaces, vectors for testing the core, and the core
- Simulation scripts, vectors, and expected results
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide