

CAST



USBHS-DEV

High Speed USB
Device Controller
Core

The USBHS-DEV core implements a complete high/full-speed (480/12 Mbps) peripheral controller that interfaces to a UTMI USB port transceiver on one side and to a system's microprocessor on the other. It is user-configurable for up to 15 IN and 15 OUT endpoints, and includes power management and remote wake-up functions.

Options include a protocol aware DMA controller, support for a variety of widely used bus interfaces, and a UTMI Low Pin Interface (ULPI).

Designed for easy reuse in ASIC and FPGA implementations, the microcode-free design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset.

Applications

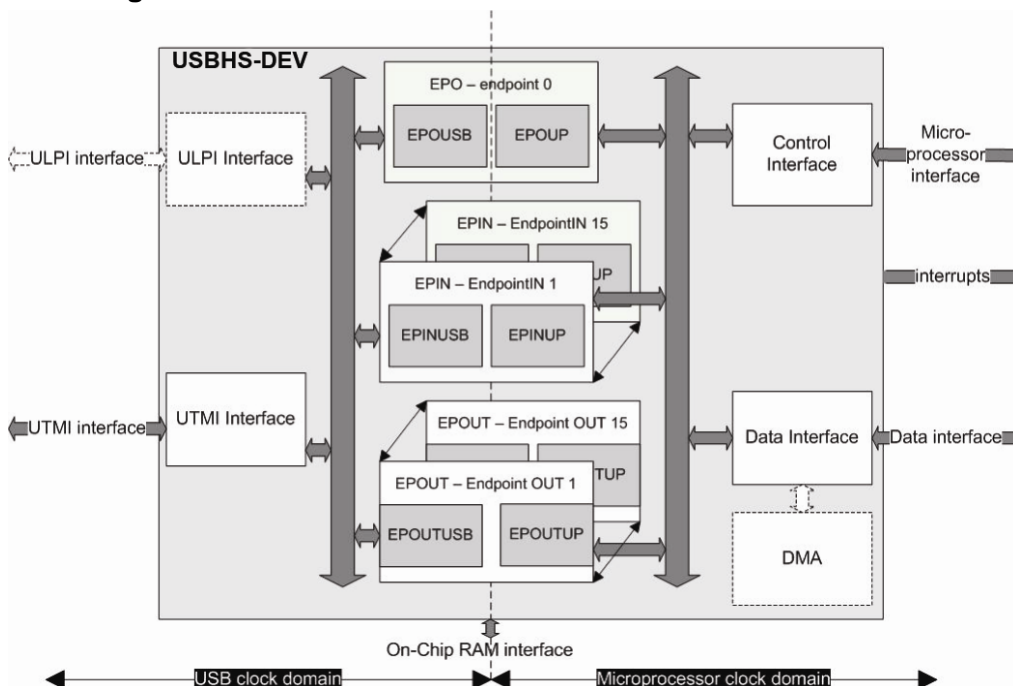
The core can be utilized in a variety of serial interface applications including:

- Embedded microcontroller systems
- Communication & networking systems
- Digital Media controllers

Software

A complete software stack configurable for the most popular device class is available. It has been designed for portability in a variety of embedded applications. It includes an intuitive Application Programming Interface (API) for application development.

Block Diagram



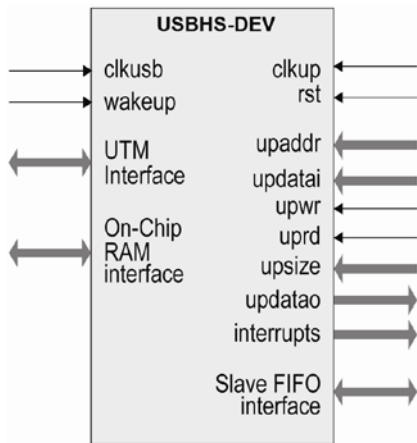
Features

- Full compliance with the USB 2.0 specification
- Control endpoint 0 — fixed 64 Bytes size
- Configurable for up to 15 IN and 15 OUT endpoints
 - Configurable/programmable number and size of endpoints
 - Configurable/programmable single, double, triple or quad buffering
 - Programmable type of endpoints
- UTMI Transceiver Macrocell Interface; Optional UTMI Low Pin Interface (ULPI)
- Choice of different microprocessor interfaces:
 - AMBA® AHB
 - PVICI
 - Generic
- Configurable 8-, 16-, or 32-bit microprocessor interface
 - Easy integration with a wide range microprocessors and bus architectures
 - Interrupt request signals for application microprocessor
 - Interrupt vector for autovectored interrupts
- Direct access to the endpoint buffers via configurable 8-, 16-, or 32-bit Slave FIFO interface
- Ready for external DMA module
- Synchronous RAM interface for FIFOs
- Optional protocol-aware DMA controller with configurable number of channels
- Suspend and resume power management functions
- Remote Wake-Up function
- Optional software stack
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)



Customer products using this core have received USB-IF certification

Symbol Diagram



Implementation Results

The following are typical performance and utilization results using Lattice ispXPGA™ devices. The first results shown are for a minimum configuration that includes one IN and one OUT endpoint.

Lattice Device	LUT4s	Registers	PFUs	SysMEM EBRs	External I/Os	Fmax (MHz)
LFX500C-4	4694	1101	1236	10	223	29.7

The next results shown are for a typical minimum configuration that includes endpoint 0 and two additional single buffered endpoints, IN and OUT, as might be used for a USB mass storage device.

Lattice Device	LUT4s	Registers	Slices	BRAM	PIOs	Fmax (UTMI / uP) (MHz/MHz)
LFEC6-3	3203	1167	2076	4	181	30/51
LFE2M35E-7	2153	932	1520	8	252	103/85

Customization

Options available upon request before delivery:

- Microprocessor Interface
- ULPI transceiver interface
- Protocol-aware DMA controller

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core includes everything required for successful implementation:

- Post-synthesis EDIF netlist (firm core) optimized for a specific Lattice device (HDL RTL source code (soft core) is also available)
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Simulation script, vectors, and expected results
- Synthesis (soft) or place and route (firm) script
- Comprehensive user documentation