

CAST



USBFS-DEV

USB Full-Speed Device Controller Core

The USBFS-DEV is a USB Device Controller that provides USB full and low speed function interface that meets the 2.0 revision of the USB specification. The USBFS-DEV logic handles bytes transfer autonomously and bridges USB interface to a simple read/write parallel interface. The USBFS-DEV can be customized and optimized for a specific application. It contains a set of Special Function Registers that is similar to the Cypress EZ-USB™ FX chip.

The microcode-free design was developed for reuse in ASICs and FPGAs. The design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset. Scan insertion is straightforward.

Applications

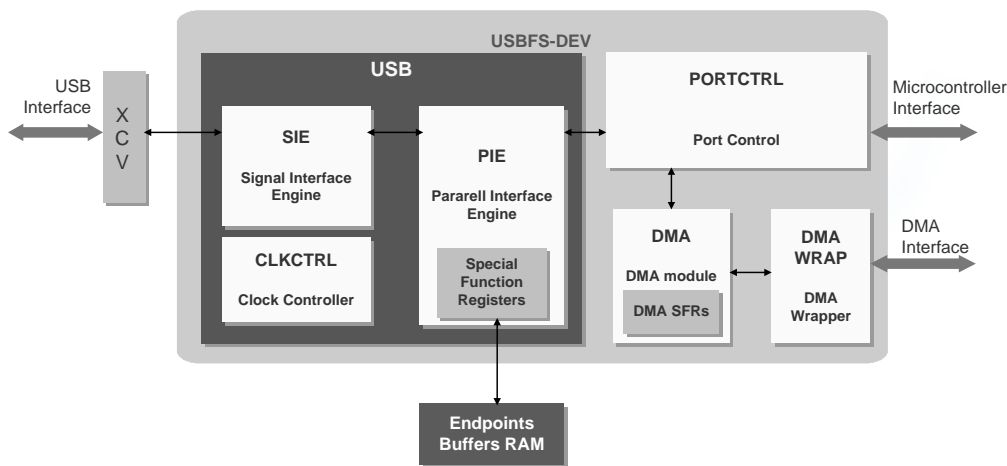
The USBFS-DEV can be utilized to provide a USB full speed function interface in a variety of applications including:

- Mass storage
- Audio
- Communication devices
- Digital cameras
- Networking
- Digital media controllers

Software

A complete software stack configurable for the most popular device class is available. It has been designed for portability in a variety of embedded applications. It includes an intuitive Application Programming Interface (API) for application development.

Block Diagram



Features

- Support for Full and Low Speed operation according to the USB 2.0 specification
- Generic system bus interface
- Serial Interface Engine
 - Support full speed devices
 - Extraction clock and data signals in internal DPLL
 - NRZI decoding/encoding
 - Bit stuffing/stripping
 - CRC checking/generation
 - Interface for an external transceiver
- Up to 31 configurable endpoints
 - Support control transfers by endpoint 0
 - Support bulk, interrupt and isochronous transfers
 - Double buffering for isochronous endpoints
 - Programmable double buffering for bulk and interrupt endpoints
- Automatic data retry mechanism
- Data toggle synchronization mechanism
- Suspend and resume power management functions
- Remote Wake-Up function
- Endpoint buffers RAM interface
 - Up to 2 x 1024 byte FIFO size for double buffered isochronous endpoints
 - Up to 64 Bytes buffer size for each bulk, interrupt and control endpoints
- Microcontroller interface
 - 8-bit data bus interface
 - Interrupt request signals for application microcontroller
 - Interrupt vector for autovector interrupts
- DMA (optional)
 - Up to 32-bit address bus width
 - 8/16/32-bit configurable data bus width
 - Big or little endian byte ordering

Optional Features

- Software stack
- On-Chip Peripheral Bus interface

Functional Description

The USBFS-DEV core is partitioned into modules as shown in the block diagram and described below:

Serial Interface Engine (SIE)

The SIE logic contains a Digital Phase Locked Loop (DPLL) that uses 4 times over-sampling of the USB data stream for clock extraction. The SIE performs serial data decoding/encoding, bit stuffing/stripping and CRC checking/generation. Received/transmitted data are grouped in bytes and transferred to/from the USBFS-DEV endpoint buffer RAM.

Parallel Interface Engine (PIE)

The PIE contains a set of Special Function Registers (SFR) that are provided to control the USBFS-DEV behavior, the logic that handles all USB transfers and interfaces for endpoints buffers and for the microcontroller.

Port controller (PORTCTRL)

The port control module contains multiplexers and address decoders. The PORTCTRL logic handles all microprocessor and DMA read and write accesses to/from the Special Function Registers and endpoint buffer RAM.

DMA

The DMA module transfers byte data between endpoint buffers and external memory. The processor initializes the DMA by writing to the DMA Special Function Registers.

DMA wrapper (DMA WRAP)

The DMA wrapper generates read/write strobes for external asynchronous RAM.

Clock controller (CLKCTRL)

This module is provided to support suspend-resume control. The clock control logic uses a clock gate to switch off the USBFS-DEV clock in suspend state.

Configurability

The following parameters allow adjusting the USBFS-DEV core to meet the requirements of the target application:

- DMA existence
- Up to 14 configurable bulk endpoints
- Up to 16 configurable isochronous endpoints
- DMA address bus width – 8/16/24/32-bit
- DMA data bus width – 8/16/32-bit
- Big or little endian byte ordering

Implementation Results

USBFS-DEV reference designs have been evaluated in a variety of technologies. The following are sample Lattice results for a minimum configuration which includes one BULK IN and one BULK OUT endpoint.

Lattice Device	LUT4s	Registers	PFUs/Slices	SysMEM EBRs	External I/Os	Fmax (MHz)
LFX200C-4	2086	619	551	6	48	71
OR4E02-3	1820	466	256	4	58	67
LFXP10C-3	1159	457	669	2	48	69
LFE2-50E-7	979	501	685	1	50	48
LFSC3GA25-7	927	502	592	1	50	48

Verification

The core has been verified through extensive simulation using a large set of test vectors and reference results, and through rigorous code coverage measurements. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

Support

The core as delivered is warranted against defects for three years from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Lattice version includes:

- Post-synthesis EDIF netlist
- Sophisticated HDL Testbench including external endpoint buffers, models of interfaces, and the core
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide

Related Products

USBFS-51 – a USB 2.0 device software stack designed to take full advantage of the 8051 Instruction Set Architecture (ISA) compliant microcontroller as well as the USB Full Speed Controller.

- **USB Full Speed Development Platform** – a complete System-on-Chip solution that integrates the previous-generation R8051XC microcontroller with the USBFS-DEV Controller, while the complementary USBFS-51 software stack and a proprietary evaluation board further facilitate application development and FPGA prototyping processes.