CAST

UDPIP-1G/10G

UDP/IP Hardware Protocol Stack Core

Implements a UDP/IP hardware protocol stack that enables high-speed communication over a LAN or a point-to-point connection. Designed for standalone operation, the core is ideal for offloading the host processor from the demanding task of UDP/IP encapsulation and enables media streaming with speeds up to 10Gbps even in processor-less SoC designs.
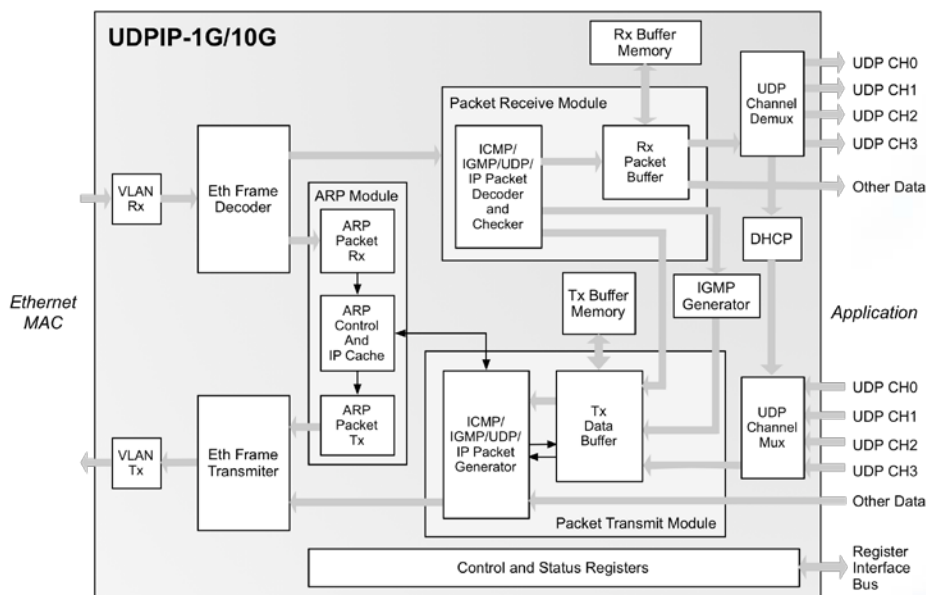
Trouble-free network operation is ensured through run-time programmability of all the required network parameters (local, destination and gateway IP addresses; UDP ports; and MAC address). The core implements the Address Resolution Protocol (ARP), which is critical for multiple access networks, and the Echo Request and Reply Messages ("ping") of the Internet Control Message Protocol (ICMP) widely used to test network connectivity. It can use a static IP address or automatically request and acquire an IP address from a Dynamic Host Configuration Server (DHCP) server. Furthermore, the core supports 801.1Q tagging, and is suitable for operation in a Virtual LAN.

The core is easy to integrate in systems with or without a host processor. Packet data can be read/written to the core via dedicated streaming-capable interfaces, or optionally via registers mapped on an SoC bus. The AMBA® AXI4-stream or the Avalon®-ST streaming protocols and the AMBA AHB and AXI, Avalon-MM, or Wishbone SoC bus protocols are supported. The core is Ethernet MAC-independent, but is available pre-integrated with a CAST, Altera, Xilinx, or other third-party eMAC core.

Applications

Video, image and audio streaming or broadcasting over Ethernet, in devices such as IP cameras compatible to the GigE Vision, ONVIF, or PSIA standards, VOIP and smart phones. Also high-frequency trading systems, high-speed communication between LAN nodes, device monitoring, and control over IP networks.

Block Diagram

Features

Complete UDP/IP Hardware Stack

- 10/100/1000 and 10G Ethernet
- IPv4 support without packet fragmentation
- Jumbo and Super Jumbo Frames
- Transmit and Receive
- ARP with Cache
- ICMP (Ping Reply)
- IGMPv3 (Multicast)
- UDP/IP Unicast and Multicast
- UDP Port Filtering
- UDP/IP Checksums generation and validation, and optional Ethernet CRC validation
- VLAN (IEEE 802.1Q) support
- Up to four UDP channels
- Ethernet Framing processing for non-UDP user-provided packets
- DHCP client

Trouble-Free Operation

- Run time programmable network parameters
  - Local, Destination and Gateway IP address
  - Source and destination UDP ports
  - MAC address
- ARP support for operation in networks with Dynamic IP allocation

Easy SoC Integration

- Flexible packet data interface:
  - Configurable 32- or 64-bit streaming capable using Avalon-ST or AXI4-Stream, or
  - Optional 32- or 64-bit AHB, AXI, Avalon-MM or Wishbone SoC buses
- Control/Status interface with optional 32-bit AHB, AXI, Avalon-MM or Wishbone SoC buses
- Separate clock domains for packet processing and control/status interfaces
- Configurable buffer sizes
- Rich interrupt support for system events
- Available pre-integrated with:
  - Altera, Xilinx, or other third-party 1G and 10G eMAC cores
  - CAST Image and Video compression cores

March 2016

Functional Description

The UDPIP-1G/10G core receives and transmits UDP packet data, and forwards other traffic from the Ethernet MAC to the application and vice versa. It also receives and transmits ARP requests and responses, and responds to ICMP echo reply messages. The core generates and validates the UDP and IP checksums of outgoing and incoming packets, respectively. It can be programmed to discard or forward corrupted packets to the user application.

The core consists of the following modules:

The **Ethernet Frame Decoder** receives Ethernet frames from an external Ethernet MAC, detects the frame type and sends frames to the ARP or the IP packet decoder. The **Ethernet Frame Transmitter** provides the external Ethernet MAC interface. The transmitter also multiplexes ARP and IP transmit packets from the core subsystems.

The **VLAN Receiver** receives Ethernet frames from an external Ethernet MAC, and when enabled detects and compares VLAN tag & filters frames to the correct VLAN tag. The **VLAN Transmitter** receives Ethernet frames from the Ethernet Frame Transmitter and adds the VLAN Tag to the frames when enabled.

The **Packet Receiver Module** receives IP packets and handles them according to the packet type. The **Packet Decoder** receives IP packets and the decoded packets are stored in the Rx Packet Buffer and then passed to the user application. The **Received Packet Buffer** implements separate data storage for the UDP application data and other data, and its size is configurable at synthesis time.

The **Packet Transmit Module** assembles UDP and ICMP packets. The UDP application data as well as the ICMP packet data are stored in the transmit buffer, the size of which is configurable at synthesis time.

The **ARP Module** sends and receives ARP packets and handles the packets according to command in the packet. The **DHCP Module** automatically requests and acquires an IP address from a DCHP server.

The **UDP Channel Demultiplexer** receives UDP packets and demultiplexes them according to a decoded UDP channel number. The **UDP Channel Multiplexer** receives UDP packet channels from a user application and multiplexes them to the Packet Transmitter module.

Finally, the **Control and Status Registers** controls the core functionality and reports the core status

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Implementation Results

UDPIP-1G/10G reference designs have been evaluated in a variety of technologies. The following are sample ASIC pre-layout results reported from synthesis with a silicon vendor design kit under typical conditions, with all core I/Os assumed to be routed on-chip. The sample results do not represent the highest speed or smallest area for the core.

UDP Channels	ASIC Technology	Eq. NAND2 gates	Fmax (MHz)	Memory (Bytes)
1	TSMC 65nm	28,926	333	16,640
1	TSMC 90nm	26,782	333	16,640
4	TSMC 65nm	36,308	333	24,832
4	TSMC 90nm	33,594	333	24,832

Table 1: UDPIP-1G/10G Sample Results for the core configured with a 32bit data-path (suitable for 1Gbps), ARP, ICMP, IGMP, Rx and Tx

UDP Channels	ASIC Technology	Eq. NAND2 gates	Fmax (MHz)	Memory (Bytes)
1	TSMC 65nm	39,181	333	33,024
1	TSMC 90nm	36,961	333	33,024
4	TSMC 65nm	48,528	333	49,408
4	TSMC 90nm	45,625	333	49,408

Table 2: UDPIP-1G/10G Sample Results for the core configured with a 64bit data-path (suitable for 10Gbps), ARP, ICMP, IGMP, Rx and Tx

Deliverables

The core is available in synthesizable RTL and FPGA netlist forms, and includes everything required for successful implementation, including a sophisticated self-checking testbench, simulation scripts, test vectors, and expected results, synthesis scripts and comprehensive user documentation.

Related Cores

Get SoC development and performance benefits by combining this UDP/IP-1G/10G Stack Core with any of these additional CAST cores:

- [EMAC-1G](): Gigabit Ethernet Media Access Controller Core
- [H2642RTP](): Hardware RTP stack for H.264
- [Image and Video Compression IP cores](): H.264/AVC video, JPEG 2000, MPEG2, JPEG, and more.

Contact CAST Sales to discuss how our IP integration services can save you even more time with any of these multi-core combinations.