

CAST

SPI_MS

Serial Peripheral Interface Master/Slave Core

Features

- Run-time programmable master or slave mode operation
- High bit rates
- Bit rates generated in Master mode:
 $\div 2, \div 4, \div 8, \div 10, \div 12, \dots, \div 512$ of the system clock
- Bit rates supported in slave mode: $f_{SCK} \leq f_{SYCLK} \div 4$
- Eight Slave Select lines
- Eight Chip Select lines
- Configurable RX and TX FIFOs
- Little or Big Endian byte mapping in multi-byte frames
- Technology independent HDL source code (soft core)
- Optimized netlist for Actel, Altera, Lattice, and Xilinx devices also available (firm core)

Designed for High Quality

- Robust verification includes integrated testbench environment and example tests cases
- Scan-ready design architecture
- Fully synchronous design with one clock domain

Applications

- Communication with Flash Memories
- Embedded microprocessor and SOCs
- Consumer and professional audio/video

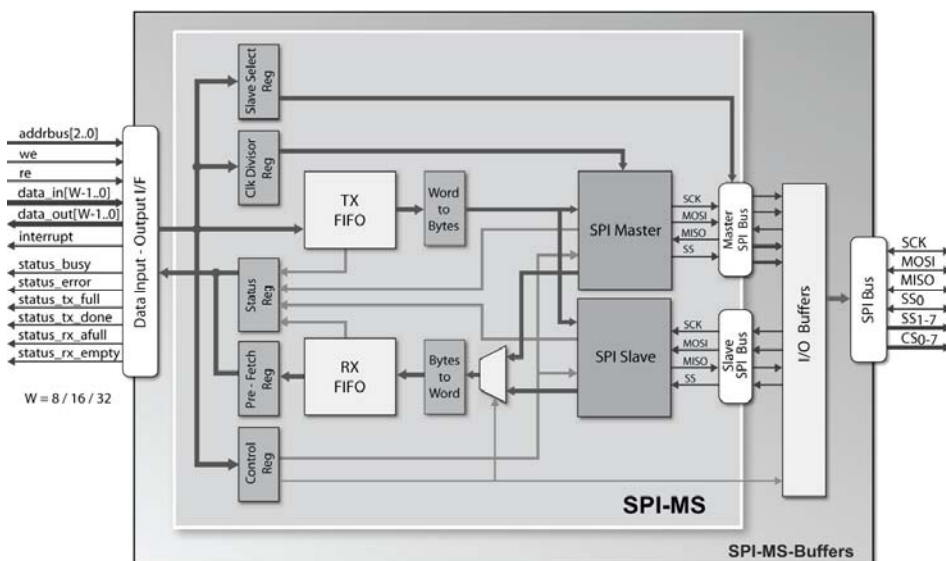
The Serial Peripheral Interface (SPI) allows high-speed synchronous serial data transfers between microprocessors, microcontrollers and peripheral devices. The SPI_MS core implements the Serial Peripheral Interface, which can operate either as a master or as a slave.

When operating in master mode, the core generates the serial data clock (SCK) and selects the slave device, which will be addressed. The master is able to generate single-byte or multi-byte frames. The internal data path of the core is configurable to 8, 16 or 32-bit width. When using a wider than 8-bit data-path, the core is able to generate partial word transfers, by generating frames with less bytes than the data path width. In this manner the core can transmit a data stream with length that is not a multiple of the data-path width.

When operating in slave mode, another master device generates the serial data clock and activates the slave select input of the core, in order to communicate. The slave is able to split the received data in partial words, in the case that a smaller than the data-path width frame is received. The slave incorporates mechanisms to reject input noise from the SPI bus, achieving a reliable data reception. Transmitted data are also accurately synchronized with the Serial Clock of the SPI bus.

The core was carefully designed to provide the most reliable communication possible, and to achieve very high bit rates.

Block Diagram



Functional Description

The SPI slave was carefully designed to provide the most reliable communication possible. In order to avoid erroneous triggering of the internal shift register caused from noise or glitches on the serial data clock (SCK) line, the SCK line is sampled and synchronized with the system clock. Special design techniques were used to obtain a reception mechanism immune against metastability errors, which would cause reception faults. Thus the reception mechanism of the SPI slave can operate reliably with a serial data clock frequency up to 1/4 of the system clock. This permits higher transfer rates when the core is used with a low frequency system clock.

The core was also designed to achieve very high bit rates. 22 Mbit/s were achieved in lab tests with the core implemented in an FPGA device and off-chip connection between master and slave. Higher bit rates are possible with faster devices and careful PCB design.

The core includes two configurable size FIFOs, one for receiving and one for transmitting. These help achieving high throughput data transfers with less host microprocessor interaction. An interrupt generation mechanism is included in the core, to provide an effective interface with a host microprocessor.

Another feature incorporated in the core is the support for eight Slave Select lines used to access up to eight devices when working as a master, as well as eight Chip Select lines.

The design is fully synchronous and has one clock domain, the system clock. This leads to a more reliable and trouble-free synthesis and implementation of the core.

Implementation Results

SPI_MS reference designs have been evaluated in a variety of technologies. The following are sample ASIC results with the core configured for 16-bit data path and 2 FIFOs (RX/TX) of 64x18 bits.

ASIC Technology	Fmax (MHz)	Logic Area ¹ (µm ²)	Number of eq. gates ²	Memory (SRAM bits)
TSMC 0.18 µm	350	43,100	4,320	2x64x18
TSMC 0.13 µm	420	20,730	4,070	2x64x18
TSMC 0.09 µm	520	10,560	3,740	2x64x18

¹ Excluding memory

² Equivalent gate count uses the smallest NAND2 gate available for the technology used

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. It has also been verified in a prototyping FPGA board platform.

Deliverables

The core includes everything required for successful implementation:

- VHDL or Verilog RTL source code
- Post-Synthesis EDIF (netlist release)
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Simulation and synthesis scripts
- Place & Route scripts (netlist release)
- Comprehensive user documentation, including detailed specifications and a system integration guide