



QSPI-APB

Quad-Bit SPI Master-Slave Controller

The Serial Peripheral Interface (SPI) allows high-speed synchronous serial data transfers between microprocessors, microcontrollers, and peripheral devices. The QSPI-APB core implements a controller for a single- or quad-lane Serial Peripheral Interface bus, which can operate either as a master or as a slave.

Designed to work with a wide variety of SPI-bus variants, the core supports different serial transfer (frame) formats. For example, the inter-frame delay, bit-width of frame and most-significant bit position in a frame are all software programmable. In master mode the core can control up to four slaves. A software-controllable clock generator derives the serial clock for master mode, by dividing the frequency of a clock line dedicated for that purpose. Under slave mode the core receives the serial clock. The master and slave clock domains are designed to be asynchronous to each other.

The controller core interacts with the host processor via an 32-bit APB slave interface that allows access to the transfer data, the control, and states registers. The APB clock is asynchronous to the SPI clocks. To ease integration, an interrupt can be generated to indicate availability of received data or availability to transmit new data. The QSPI-APB implements two 16-word FIFOs, one for the receiver and one for the transmitter path, and handshaking signals to ease operation with an external DMA controller.

The QSPI-APB core is proven and available in RTL source or as a targeted FPGA netlist.

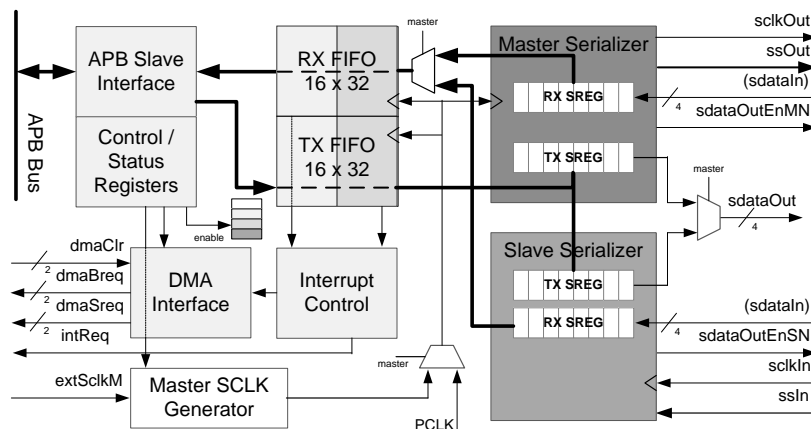
Applications

The QSPI-APB core is suitable for implementing serial interfaces in a wide range of applications, including host communication with flash memories, and peripherals such as sensors, ADC/DACs, touchscreens, video game controllers, and audio/video codecs.

Support

The QSPI-APB as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Block Diagram



Features

Flexible SPI Master/Slave

- Single- or Quad-Bit Serial Interface
- Up to four slaves under Master control; four slave-select lines of programmable polarity
- Configurable frame format
 - 4 to 32 bit frames
 - Configurable inter-frame delay
 - MSB-first and LSB-first frames
- Separate clock input and scaler for master serial clock generation
- Asynchronous Master and Slave interfaces

Easy Integration

- 32-bit AMBA/APB interface
- Asynchronous SPI and APB clocks
- 16 word Tx and Rx FIFOs and DMA controller handshaking signals
- Software programmable operation
- Maskable interrupt and status registers for status reporting

Smooth Technology Mapping

- Fully synchronous, scan-ready design architecture
- Delivered with sample scripts, RTL test-bench and sample test-cases