

CAST

PCI-T64

64-bit/66MHz PCI Target Interface Core

Features

- Flexible VHDL synthesizable core
- PCI specification 2.3 compliant
- 66 MHz performance
- 64-bit data path
- Zero wait states burst mode
- Target functionality
- Single interrupt support
- Type 0 Configuration space
- Support of all Base Address Registers
- Support of backend initiated target retry, disconnect and abort
- Parity generation and parity error detection

The main purpose of the PCI-T64 Interface Core is to isolate the user from having to solve complex problems of PCI interface implementation and let the user focus on the application development.

The PCI-T64 Interface supports a 64-bit address/data bus and operates at up to a 66MHz (PCI clock frequency). It is fully compliant with the PCI Local Bus Specification, Revision 2.3.

The Target supports up to six Base Address Registers with both I/O and Memory space decoding from 16 bytes up to 4GB.

Target supported commands are:

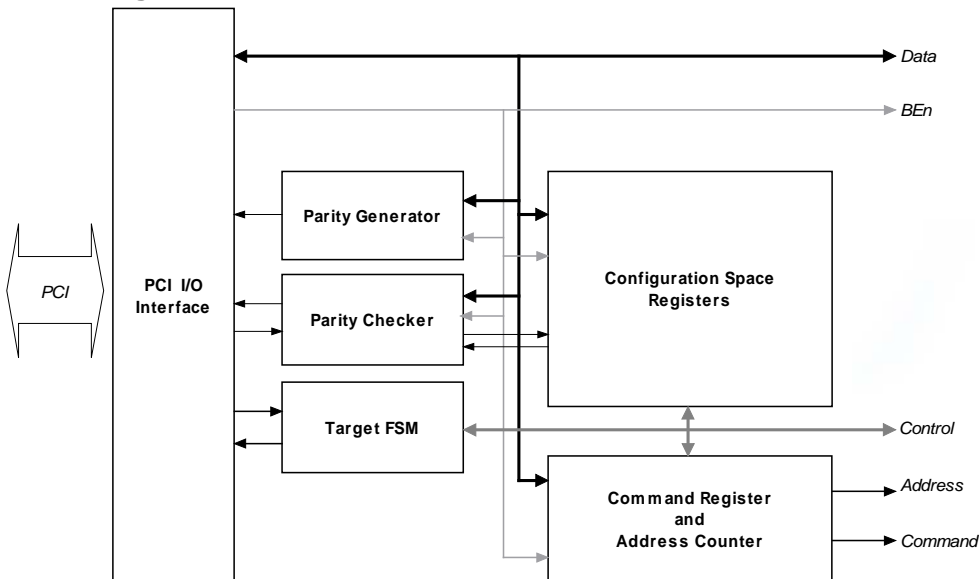
- Configuration Read, Configuration Write
- Memory Read, Memory Write, Memory Read Multiple (MRM), Memory Read Line (MRL),
- I/O Read, I/O Write

Applications

The PCI-T64 can be utilized in a variety of PCI Interface applications including:

- PCI I/O communication boards
- PCI Data Acquisition Boards
- Embedded system PCI applications

Block Diagram



Functional Description

As shown in the Block Diagram and explained below, the PCI-T64 includes six major blocks: PCI I/O Interface, Parity Generator, Parity Checker, Configuration Space Registers, Command Register and Address Counter block, Target State Machine.

PCI I/O Interface

The Interface block is responsible for the interface with the PCI Bus. The block implements I/O buffers and I/O registers.

Parity Generator

The parity generator generates parity during read transaction.

Parity Checker

The parity checker checks parity during command phase and write transaction.

Configuration Space Registers

Configuration Space Registers block implements the mandatory 64 bytes of PCI Configuration Space registers. See the chapter PCI Configuration Space for more details.

Target FSM

Target State Machine is a control block of the PCI-T64 interface. The state machine is in charge of handling PCI transactions protocol.

Core Configuration

The customer can adjust the PCI-T64 core parameters in the VHDL source. For the netlist license the delivered netlist is generated with the parameters specified by the customer.

Please contact CAST for any required information.

Implementation Results

PCI-T64 reference designs have been evaluated in a variety of technologies.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Implementation Results

PCI-T64 reference designs have been evaluated in a variety of technologies. The following are representative ASIC results for the core configured with a single base address register.

ASIC Technology	Cell Area	NAND2 Area	Approx. Area (gate equiv.)	Frequency (MHz) PCI Clock
TSMC 65 nm	5,506	1.6	3,441	66
TSMC .09 μ m	8,562	2.8224	3,000	66
TSMC .13 μ m	17,075	5.0922	3,353	66
TSMC .18 μ m	36,281	9.9792	3,635	66

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide