

# CAST



## PCI-T32

### 32-bit/33MHz PCI Target Interface Core

#### Features

- Flexible synthesizable VHDL core
- PCI specification 2.3 compliant
- 33 MHz performance (66MHz optional)
- 32-bit datapath
- Zero wait states burst mode
- Full Target functionality
- Single interrupt support
- Type 0 Configuration space
- Support of all Base Address Registers
- Support of backend initiated target retry, disconnect and abort
- Parity generation and parity error detection
- Available in synthesizable VHDL source code

The main PCI-T32 Interface core purpose is to isolate the user from having to solve complex problems of the PCI interface implementation and let the user instead focus on the application development.

The PCI-T32 Interface supports 32-bit address/data bus and operates up to 33 MHz (66 MHz optional) PCI clock frequency. It is fully compliant with the PCI Local Bus Specification, Revision 2.3.

The PCI-T32 Interface is a Target-only PCI Interface core. The interface implements 64 bytes of PCI Configuration Space registers. It is possible to extend the Configuration Space up to 256 bytes if required.

The Target supports up to six Base Address Registers with both I/O and Memory space decoding from 16 bytes up to 4 GB.

The Target supported commands are:

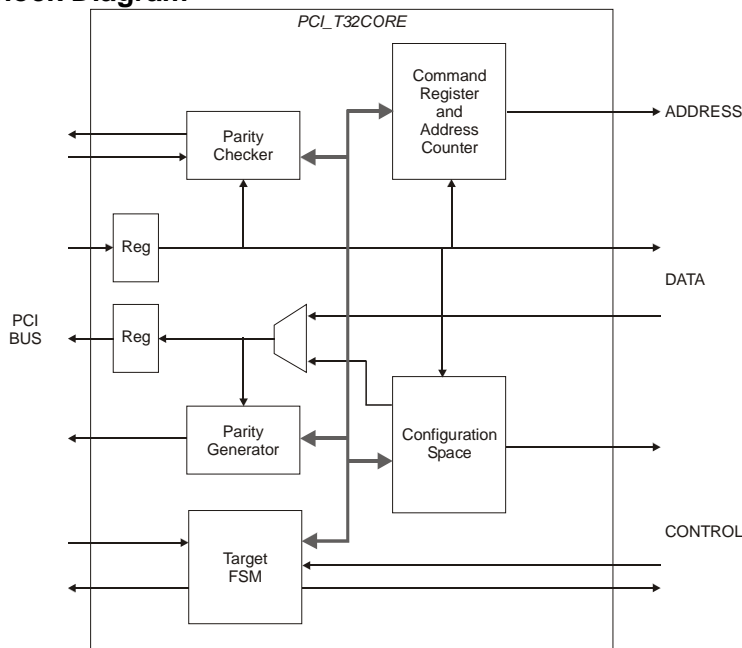
- Configuration Read, Configuration Write
- Memory Read, Memory Write, Memory Read Multiple (MRM), Memory Read Line (MRL), Memory Write and Invalidate (MWI)
- I/O Read, I/O Write

#### Applications

The PCI-T32 can be utilized for a variety of PCI interface applications including:

- PCI I/O communication boards
- PCI Data Acquisition Boards
- Embedded system PCI applications

#### Block Diagram



## Functional Description

As shown in the block diagram, the PCI-T32 includes five major blocks: Parity Generator, Parity Checker, Configuration Space Registers, Command Register and Address Counter block, Target State Machine.

### Parity Generator

The parity generator generates parity during read transaction.

### Parity Checker

The parity checker checks parity during command phase and write transaction.

### Configuration Space Registers

Configuration Space Registers block implements the mandatory 64 bytes of PCI Configuration Space registers. See the chapter PCI Configuration Space for more details.

### Command Register and Address Counter block

Command Register saves a transaction command at the beginning of PCI transaction. Address Counter block generates a backend address. Address counter is controlled by Target FSM.

### Target FSM

Target State Machine is a control block of the PCI-T32 interface. The state machine is in charge of handling PCI transactions protocol.

## Core Configuration

The customer can adjust the PCI-T32 core parameters in the VHDL source. For the netlist license the delivered netlist is generated with the parameters specified by the customer.

The PCI-T32 core can support 66 MHz PCI bus speed. Depending on the target technology a minor modification might be required.

Please contact CAST for any required information.

## Implementation Results

PCI-T32 reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results with IOBs assuming all core I/Os are routed off-chip, and with single base address register configuration for slices.

Supported Family	Slices	IOBs	BRAM	Fmax (MHz)	ISE Version
Spartan-3E 3S250E-4	206	48	0	33	12.2i
Spartan-6 6SXL16-2	99	48	0	33	12.2i
Virtex-4 4VLX25-10	167	48	0	33	12.2i
Virtex-5 5VLX40-1	115	48	0	33	12.2i

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

## Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide